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MANUFACTURING METHODS REPORT. STATIC SWITCH.(U)
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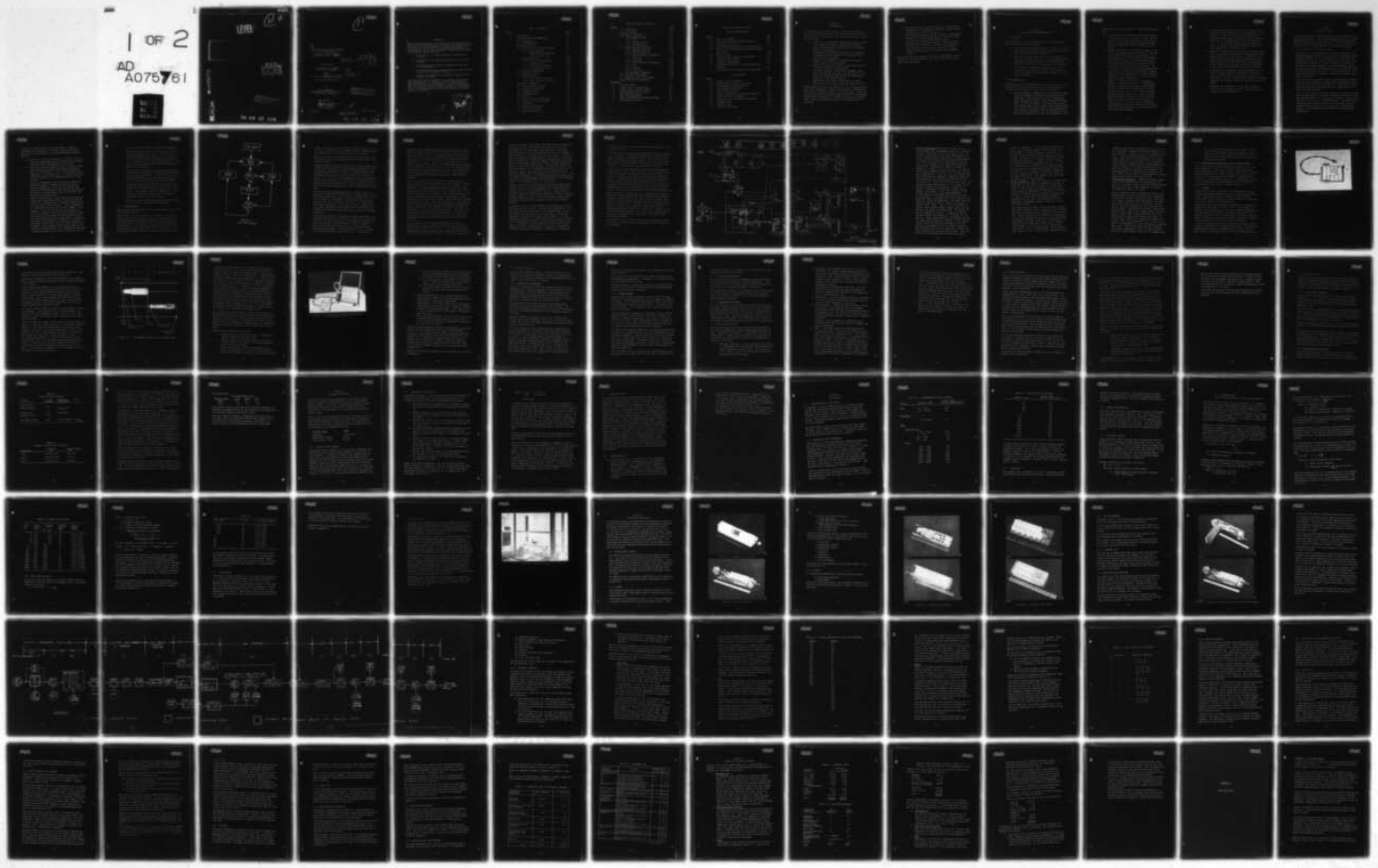

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ABSTRACT

This report covers all activity carried out under Contract NO. DAAH01-75-C-0552, "Manufacturing Techniques for Static Switches". The purpose of this contract was to improve the producibility and reliability of the present 2.75-inch rocket launcher intervalometer through the improvement of manufacturing methods and techniques brought about by:

a. Conversion of all timing functions to solid state circuits,

b. Conversion of all switching functions to solid state circuits,

c. Provision for the sensing and bypassing of any open or shorted squibs,

d. Pilot production of five prototype solid state switches to verify the techniques chosen.

e. Design of an assembly line capable of producing 1000 switches per week.

The contract has been concluded with all above tasks successfully accomplished. In addition, a reliability analysis of the solid state circuitry was conducted, an EMI analysis was made, and some EMI testing was done. A detailed investigation into the conversion of the electronic circuitry to one hybrid circuit chip was performed. All of these activities are documented in the report.

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TABLE OF CONTENTS

FMC

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

FMC

SECTION I
INTRODUCTION

The presently used sequence switch, consisting primarily of an electromechanical stepping switch, exhibits faults common to such mechanical devices used in aircraft environments. These faults include:

a. Sensitivity to shock and vibration resulting in short life, mechanical failure, and erratic operation.
b. Short life and erratic operation due to mechanical wear of component parts.
c. Degradation of electrical contacts due to moisture, corrosion, fungus, migration of lubricants, etc., which result in misfires.
d. Sensitivity to temperature extremes resulting in erratic timing of firing pulses.
e. Sensitivity to supply voltage fluctuations resulting in erratic timing of firing pulses.
f. Critical tolerances in mechanical assembly, which affect the timing, accuracy, and reliability of the switch are dependent upon the skills and variable attitudes of the human assembler.
g. Deterioration of contacts when trying to fire a shorted squib may lead to premature switch failure.

Prior studies have shown the feasibility of using solid-state electronic components to replace the mechanical components in the switch and thereby eliminate the above faults. Incorporation of solid-state electronics makes possible the development of production procedures that reduce fabrication and assembly costs. Use of solid-state circuitry will accomplish the following:

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a. Provide extremely accurate timing for firing pulses regardless of environmental conditions, supply voltage fluctuations, or age of the unit.
b. Provide self-protection against shorted or open squibs, stepping to the next available good squib and firing it within the alloted time between firings.
c. Make possible an automated assembly line with little operator skill required. Automatic test equipment incorporated in the line will analyze and reject defective units before final potting and acceptance testing.

Because of this great potential for switch improvement in both reliability and producibility, the program described in this report was undertaken.

SECTION 2
CONCLUSIONS AND RECOMMENDATIONS

2.1 CONCLUSIONS

Conclusions that can be drawn from the work performed under this contract include the following:

a. A solid-state sequencing switch is feasible and prototypes of such a switch have been designed, fabricated, and tested to verify the feasibility.

b. This switch can be mass-produced using common electronic production techniques. No unique processes or components are required and no new skills must be learned by normal electronic assembly line personnel.

c. The resultant, mass-produced switch will be more accurate, more reliable, and have a much longer life than the present electromechanical switch it is designed to replace.

2.2 RECOMMENDATIONS

Recommendations for additional work to be done prior to mass production of the solid-state switch and its introduction into the military supply system include the following:

a. Simplification of hardware for cost savings in production line assembly and added reliability should be undertaken. This simplification was investigated under the present contract and is discussed in some detail within this report. Because of the time and cost limitations of this program, these hardware simplifications could not be used for the manufacture of five prototype switches. They involve tooling costs which are acceptable only when the commitment to high-

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volume production has been made. These simplifications are:

(1) Conversion of the discrete electronic components to a hybrid circuit. This will cut the number of printed wiring boards in the switch from two to one, and drastically reduce the number of components to be machine and hand inserted into the boards.

(2) Design of a suitable, high-volume package for the toroid transformers used in the switch. For the five prototype switches the transformers (19 in each) were made by winding primary and secondary windings on a standard, easily available core. Each transformer was then hand mounted into its proper place on the printed wiring board. For high-volume production a method of packaging must be devised in which the transformers are machine wound and all encapsulated into a single drop-in package with pins spaced to fit a mating board or flexible circuit interconnect.

(3) Design of a high-volume circuit interconnect method. The major components of the prototype switches (printed wiring boards, connector and load/arm switch) are interconnected with many individual wires, each cut to length, stripped, and hand soldered into place. For high-volume production great labor savings can be realized through the use of custom designed flexible circuit wiring. With this type of wiring all connections can be made at once with no chance of miswiring, and then machine flow-soldered to complete the wiring process.

b. An investigation into the variation in output characteristics of the decoder/drivers, as described in paragraphs 3.1.3 and 3.4, should be conducted to see if the device manufacturer can provide units with guaranteed output at low temperature and at a reasonable cost. If not, an added stage of amplification might have to be added to the decoder/driver output to insure operation of all units at -55°C.

c. Methods of lowering the induced noise on unfired squib lines, discussed in paragraph 3.4, should be investigated along with a close analysis of MIS-23156 to determine whether the requirements spelled out, which were written for an electromechanical intervalometer firing squibs with dc voltage, are really applicable to the solid-state switch operating at 10 kilohertz.

d. An extensive environmental test program should be conducted on many solid-state switches, the amount of which is great enough for statistical analysis to be meaningful. The five units produced under this contract underwent only limited testing as specified by the contract.

e. Dedicated test equipment to allow rapid go/no-go testing of the switches should be developed for both production line and field use.

SECTION 3
TECHNICAL ACTIVITY

The technical activity carried out under this contract centered around the conversion of the electromechanical switch to a solid-state design through circuit design, breadboarding and testing, prototype design, fabrication and testing. Each of these areas of activity will be described in the following paragraphs.

3.1 CONVERSION TO SOLID-STATE DESIGN.

Meeting all of the specifications originally written for the electromechanical switch with a new unit of solid-state design presented a number of real challenges. The requirement for squib shorting by less than 0.1 ohm ruled out the use of any semiconductor element as a switch in series with the squib. And the 30 millisecond maximum "time-to-first-fire" requirement meant that the electromechanical switch's inherent memory of its last position, with power off would somehow have to be duplicated or designed around with presently available electronic components.

To solve the above problems, several "brainstorming" sessions were held with engineers of highly varied backgrounds, both electrical and mechanical, in attendance. Many ideas were proposed and each was investigated for its feasibility by the project design engineers.

About the only feasible method to emerge for meeting the squib shorting requirement with present technology was that of using the secondary winding of a transformer, whose dc resistance is less than 0.1 ohm, as the shorting element. Then when firing of the squib is required, energy will be coupled into this winding by application of an ac fire pulse on the primary winding. This was picked as the method to be designed and breadboarded.

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To meet the "time-to-first-fire" requirement a number of approaches were considered. A number involved solid-state duplication of the "memory" of the electromechanical switch such as:

a. Nonvolatile solid state memories and bubble memories. Both were considered too new and presently too expensive for serious consideration at this time.

b. Built-in, long life battery to keep a volatile memory alive during the required 400 cycles and whatever shelf life is necessary. This was considered to be a lessening of the reliability of a totally solid-state unit and building in an obsolescence that was undesirable.

c. Use of a programmable, read-only memory (PROM) and permanently alter the memory during each firing. Memories capable of controlling the required 400 cycles are attainable but again built-in obsolescence was felt to be undesirable since a solid-state unit should have unlimited life.

d. Magnetic memory cores. This method was a strong contender and investigation into it's possible use was carried on in parallel with the chosen method during the early part of the program. It was determined to be a feasible method but was finally dropped for two reasons. First it was felt that the circuitry involving 19 magnetic cores and their read/write amplifiers would be more costly and take up more space in the small package than the chosen method. Secondly, this method would require a deliberate "resetting" of the memory cores at the time the rocket launcher was reloaded. This resetting would require power on the circuit and would present a new and possibly dangerous reloading sequence in the field. Because of this it

was decided that this was an unacceptable approach.

The chosen approach does not duplicate the "memory" of the electromechanical switch. Instead it uses a scanning technique which locates the first unfired rocket, through sensing squib impedance, and fires it. If the switch can scan, locate a good squib, and fire it within the prescribed 30 milliseconds then a memory is not required.

The circuitry required for scanning can be designed using standard semiconductor components manufactured to military specifications. Similar circuitry has been used successfully in other applications and its use here appeared to present no unusual problems.

An added bonus with this approach is the fact that shorted and open squibs will be bypassed and a good rocket will be fired with each closure of the trigger switch. The present switch will attempt to fire a bad squib and remain in place until a command is generated to move to the next position.

For these reasons, the scanning approach was selected as the one to be designed and breadboarded.

3.1.1 Circuit Design

Actual circuit design began with the establishment of the logic flow diagram of Figure 3-1.

Upon receipt of a fire command (i.e. closure of the trigger switch which applies voltage to the unit) squib number 1 is selected and a determination is made as to whether or not it is a good squib. If not the select circuitry is advanced to squib number 2. This advancement continues until the first good squib is found. When that occurs, a fire pulse of 40 milliseconds duration is sent to the squib to fire it. After

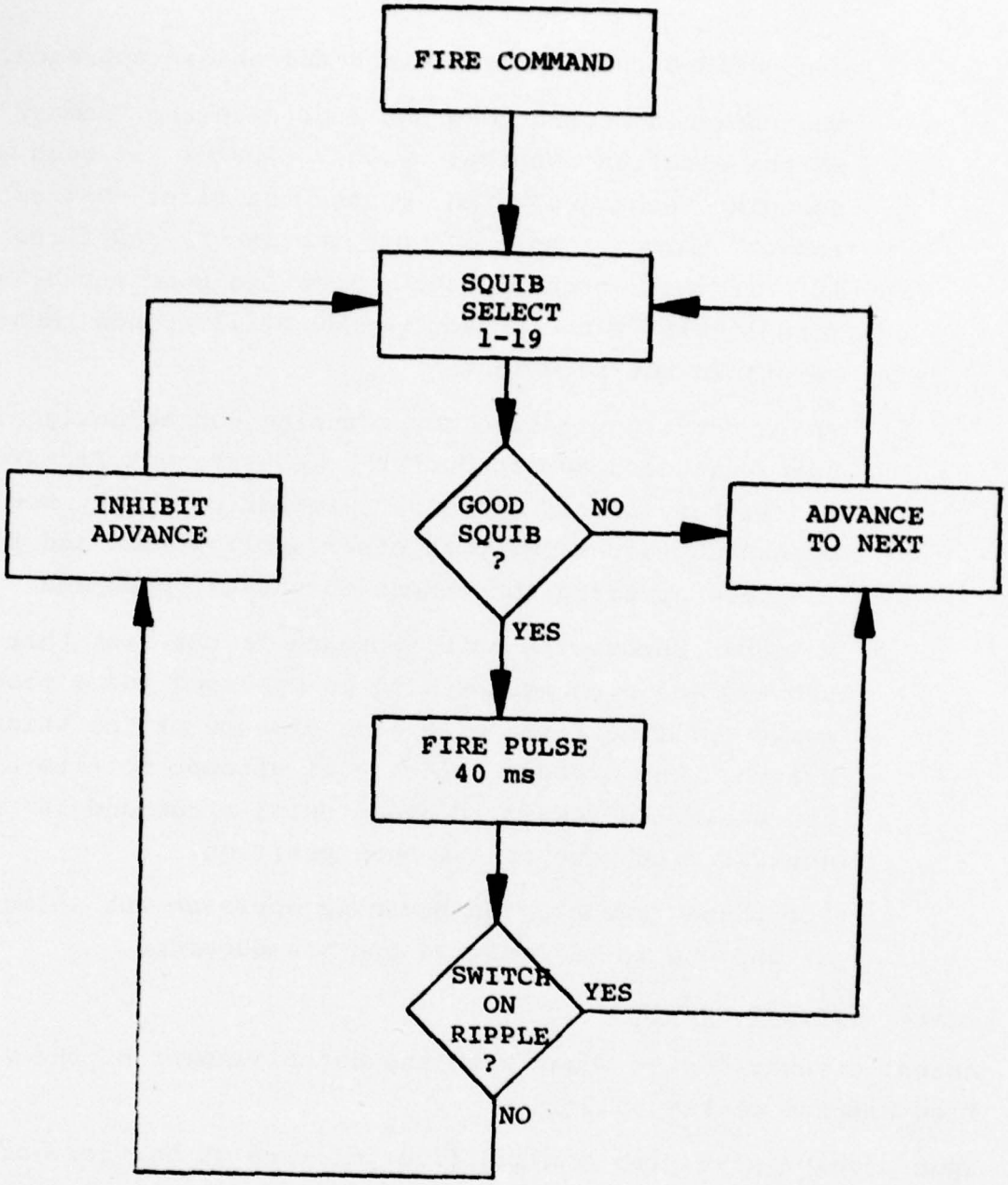


FIGURE 3-1
LOGIC FLOW DIAGRAM

firing, the squib select circuitry is either advanced to the next squib or inhibited from advancing further depending upon the setting of the ripple/single fire select switch.

Design of circuits to accomplish the logic depicted was then divided into two major areas; squib shorting and firing, and logic and timing.

3.1.1.1 Squib shorting and firing circuit design began with a concept involving individual power amplifiers for each of the 19 outputs, operating at a frequency of one megahertz, and a shorting method in which a load in the primary side of the transformer is activated to reflect back to the secondary a load of 0.1 ohm or less. The output amplifier and transformer designs were considered to be the areas of greatest concern and work was begun on them first. Active squib shorting circuitry would be incorporated after their satisfactory development.

During the initial breadboarding of the output circuit, a transformer consultant and fabricator was called upon to assist FMC with selection and source of the transformer cores. Due to the packaging requirement of small size and the digital nature of the logic circuitry, the choice of a 1 MHz square wave seemed appropriate. But because of this frequency and wave shape, problems were encountered with stray wiring capacitances and inductances and long turn-off times of switching transistors.

Since these problems at 1 MHz were not easily resolvable, the frequency was lowered to 100 kHz with significant increase in core size but still within the total package requirement if a common power amplifier were used for all the 19 outputs. Various core materials, with different permeabilities and using different numbers of turns and ratios, were tried with a conventional push-pull power amplifier. A satisfactory

amplifier using 2N2905A transistors was tested with a center-tapped 56-turn primary and 3-turn secondary ferrite toroidal core transformer. Due to the numerous interconnections necessary with 19 stations, a single-ended amplifier circuit was designed using a dc pulse driving an iron powder core transformer with 30:3 turns. Since this transformer does not require a center tap the number of interconnections were reduced to the minimum of 4 per transformer. An active squib shorting circuit was then attempted on this 100 kHz, single-ended amplifier and transformer circuit. The active squib shorting circuit consisted of steering diodes, power transistor and resistors.

Due to the coupling inefficiency (the secondary, having 3 turns, trying to drive the primary, having 30 turns), leakage inductance (secondary windings on top of the primary), and relatively high semiconductor threshold voltage, this active shorting circuit would not work at low voltage levels. So an analysis was made of the launcher wiring from the intervalometer to the rocket ignition contact to determine if such a squib shorting circuit would function considering the impedance and frequency involved. After this analysis, it was concluded that the wiring reactance and the transformer secondary would provide sufficiently high impedance to limit the current in the squib to a safe level at RF frequencies. Therefore, the active squib shorting circuit was abandoned. At dc and low frequencies, squib shorting is provided by the transformer secondary winding, whose resistance has been measured to be 0.072 ohm.

Soon afterward, it was found that MIL-STD-1385 (NAVY), "Preclusion of Ordnance Hazards in Electromagnetic Fields; General Requirements for", states: "4.1.2 Alternating power sources with frequency greater than 10 kHz shall not be used for the normal initiation of EEDs". Since one of the users of

the intervalometer is the Navy, the power output frequency was reduced to 10 kHz. This change increased the size of the transformer core sufficiently that packaging of the solid state version was to be quite difficult. Due to the longer pulse duration of a 10 kHz, 50% duty cycle pulse, it was necessary to abandon the dc pulse amplifier and turn to a modified push-pull amplifier. With this type of operation, the current level of the primary winding is reduced, thereby reducing the station select driver requirement. This modified push-pull amplifier consists of two transistors which are turned on and off out of phase. The collectors of both transistors are connected together and then capacitively coupled to each of the 19 output transformers. The modified push-pull amplifier does not require a center-tapped transformer resulting in a minimum number of interconnections to the transformer.

3.1.1.2 Logic and timing circuit design began with the squib select circuitry which was developed using two binary-coded-decimal (BCD) to 10-line decoder/drivers. These standard integrated circuits perform the function of selecting one of nineteen squibs at a time without requiring the use of nineteen discrete output circuits. A four-bit digital counter and a flip-flop provide the BCD sequencing input to the decoder/drivers.

Circuitry to sense for good squibs was developed using a dual differential line receiver. Problems were encountered in its use and accurate current sense levels corresponding to open and shorted squibs could not be established. The problem appeared to be too high an input offset voltage. No other integrated circuits with better characteristics could be found so a current sense circuit was designed using discrete components. Transistor and diode junction voltages were used to establish current sensing levels. Temperature compensation circuitry including a thermistor was designed to compensate

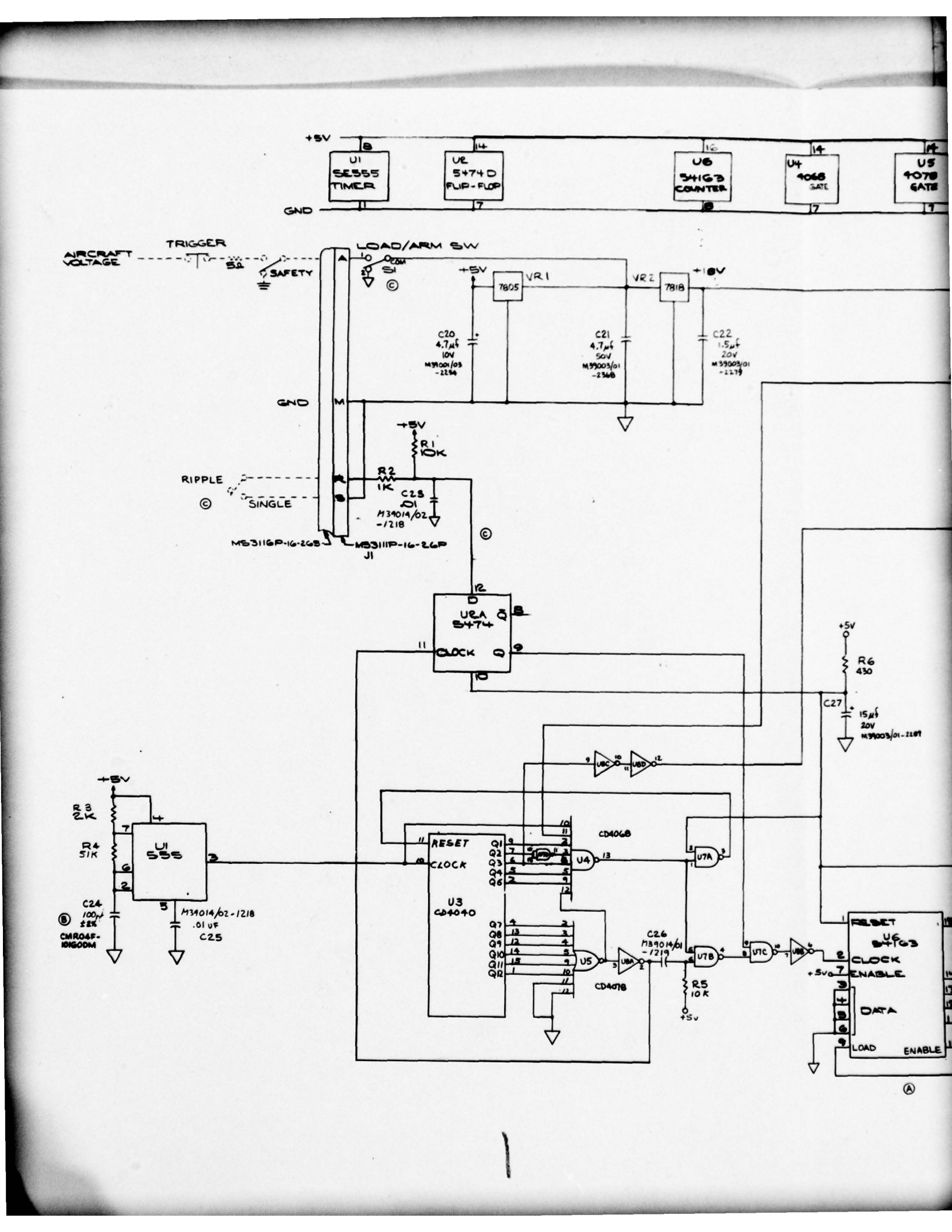
these junctions over the required operating temperature range of -55°C to 75°C.

A good squib is required by specification to have a resistance of 1 ± 0.3 ohms. Launcher wiring between the switch and the squib can exhibit a resistance ranging from .04 to .87 ohms. Thus a good squib and wiring could be from .74 to 2.17 ohms. As a result the current sense levels were chosen to indicate a short at .7 ohms and an open circuit at 2.4 ohms.

Timing circuitry was initially designed using two integrated circuit NE555 timers. One was used as a free-running oscillator which developed the output frequency and the other was used as a one-shot to provide the 40-millisecond fire pulse. Because of problems with the one-shot being triggered during circuit power-up, the design was changed to use a counter in conjunction with the free-running oscillator and count pulses equivalent to 40 milliseconds and establish the fire pulse period. This design was breadboarded and operated successfully.

When the output circuitry and logic circuitry were married together, it became apparent that additional circuitry would be required to select the precise time at which to check squib current to decide whether to remain at that output and fire or step to the next output. Another counter was originally concepted to provide this timing for sensing squib current. A scheme was developed, however, to use a single counter to provide both timing functions. This counter is a CMOS divide-by-4096 ripple counter and its operation is described in the following paragraphs.

The complete circuit design is shown in the schematic diagram of Figure 3-2. Referring to the schematic, circuit operation is as follows:


+5V
U1 SE555 TIMER
U2 5474 D FLIP-FLOP
U6 54163 COUNTER
U4 4068 GATE
U5 4078 GATE
GND
TRIGGER
AIRCRAFT VOLTAGE
50Ω
SAFETY
LOAD/ARM SW
S1
VR1
7805
VR2
7818
+18V
C20 4.7µf 10V M39001/03 -2254
C21 4.7µf 50V M39003/01 -2368
C22 1.5µf 20V M39003/01 -2279
R1 10K
R2 1K
C23 .01 M39014/02 -1218
RIPPLE
SINGLE
MS3116P-16-26S
MS3111P-16-26P
J1
U2A 5474
CLOCK
R6 430
C27 15µf 20V M39003/01-2289
U8C
U8D
R3 2K
R4 51K
U1 555
C24 100µf ±2% CMR06F-101GODM
C25 M39014/02-1218 .01 UF
RESET
CLOCK
U3 CD4040
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
CD4068
U4
U7A
U5
CD4078
U8A
C26 M39014/01 -1219
U7B
U7C
U8B
R5 10K
U6 54163
CLOCK
ENABLE
+5Vo
DATA
LOAD
ENABLE

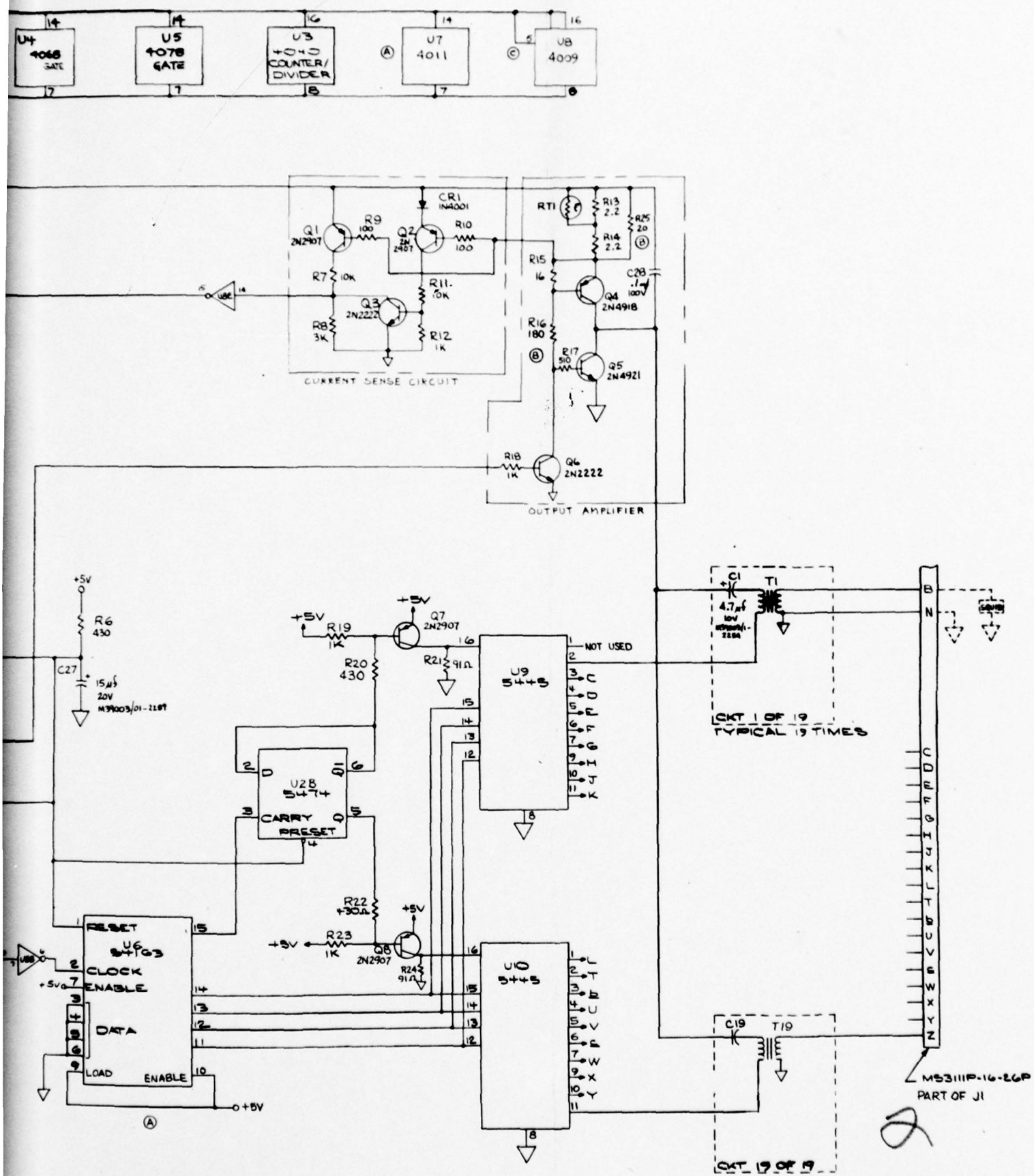


Figure 3-2. Solid-State Switch Schematic Diagram

a. Logic & Sequencing--When power is applied to pin A of the connector and the LOAD/ARM switch is in the ARM position, regulators VR1 and VR2 supply +5 Vdc and +18 Vdc respectively to the logic and amplifier circuits. Several initial conditions are established by the slow rise of voltage at the junction of R6 and C27. The Q outputs on flip flops U2A and U2B are preset high. Counter U6 is reset to a count of 0. Counter U3 is reset to 0 thru gate U7A. U6, U2B, U9, and U10 are connected to form a 1-of-20 line counter and decoder/driver. Line one of U9 is not used since only 19 outputs are required. Resetting counter U6 and presetting flip flop U2B selects line 1 of 20. U1 is connected as a free running 80 kHz oscillator, and provides overall system timing. It's output is connected to counter U3 and gate U4. Output Q3 of counter U3 provides a 10 kHz drive signal, through buffers U8C and U8D, to the output amplifier. No current flows thru the output amplifier with line 1 of 20 selected. A current sense circuit monitors the amplifier current and generates a low output when the amplifier current is above or below a good squib's current level. When line 1 of 20 is selected the current sense circuit senses an open circuit and generates a low output to inverter U8E. The output of U8E is connected to gate U4. In addition gate U4 receives inputs from counter U3, oscillator U1, and gate U5. These inputs establish the precise time when the output squib current is checked. If the current is not correct at this time the output of U4 will pulse low and counter U3 will be reset by gate U7A. U7B will pulse U7C, U7C will pulse U8B, and U8B will clock counter U6 to the next higher count. Line 2 of 20 will now be selected and the first real squib

circuit is selected. If a good squib is sensed the output gate U4 will not pulse low and counter U3 will not be reset. It will continue to count until it reaches a count of 4096. Then the output of U5 will go high, the output of U8A will go low and clock flip flop U2A and pulse U7B. Clocking U2A will transfer the SINGLE/RIPPLE fire information to U7C. If a low is transfered to U7C, SINGLE fire has been selected and the gate will be disabled preventing the clocking of counter U6. If a high is transfered, RIPPLE fire has been selected and counter U6 will be clocked to the next higher count. The sequence will then repeat if RIPPLE fire has been selected.

b. Output Circuitry -- Buffer U8D applies a 5 volt 10 kHz square wave to R18 which is connected to the base of transistor Q6. When the collector of Q6 goes low, Q5 turns off and Q4 turns on supplying current to the output coupling capacitors, C1 through C19. When the collector of Q6 goes high, Q4 turns off and Q5 turns on sinking current from the coupling capacitors. Resistors R13, R14, R25, and thermistor RT1 form a temperature compensated current element for the current sense circuit.

Each decoder/driver output line has an open collector NPN output transistor with a substrate diode connected between the collector and the emitter of that transistor. When an output line is selected, the transistor turns on and switches the primary of the corresponding transformer to ground. When line 2 of decoder U9 is selected and the amplifier output is high, current flows through C1, the primary of T1, and the NPN transistor of line 2 in the decoder. When the amplifier output is low, it sinks current through the same

elements except that the substrate diode in line 2 of U9 provides a reverse current path instead of the NPN transistor. Capacitor C1 is an ac coupling capacitor. Each transformer primary is coupled to the output amplifier by its own capacitor. The transformer turns-ratio is such that a 15 volt peak-to-peak square wave applied to the primary produces an output of about 3 volts peak-to-peak to the squib when that primary is selected by the decoder. The dc resistance of the secondary is designed to be less than 0.1 ohm to meet the squib shorting requirement when the squib is not being fired.

c. Current Sense Circuitry -- Amplifier output current flows thru thermistor RT1 and resistors R13, R14, and R25. When the voltage across the series-parallel combination exceeds .6 Vdc transistor Q1 turns on and supplies current to R7 and R8.

When it exceeds 1.2 Vdc, transistor Q2 turns on and supplies base current to transistor Q3. Transistor Q3 shunts the current flowing thru R8 to ground and a low input to inverter U8E is produced. Thus when the voltage across RT1, R13, R14, and R25 is less than .6 Vdc all transistors Q1, Q2, and Q3 are off and the input of inverter U8E is tied to ground thru R8 and is low. This is the "open circuit" condition. When a voltage above .6 Vdc is present only Q1 is turned on and a high is produced at the input to inverter U8E. This is the "good squib current" condition. When a voltage greater than 1.2 Vdc is present, all transistors are on and the input to inverter U8E is low. This is the "short circuit" condition. The circuit arrangement of RT1, R13, R14, and R25 produces a higher output voltage at low temperatures,

for a given amplifier current, and a lower output voltage at high temperatures to compensate for variation in the turn-on voltages for the base-emitter junctions of Q1 and Q2 and diode junction of CR1 over the temperature range.

3.1.2 Breadboard and Engineering Test Unit Fabrication

The circuits designed were converted to hardware in the form of a breadboard - a unit that can easily be modified and tested during the final design stages. Tests were conducted, minor modifications were made, and when it was felt that the entire circuit was operating as desired the breadboard was converted to an engineering test unit - a hardwired unit which can be handled and put through temperature and field tests. This engineering test unit is shown in Figure 3-3.

3.1.3 Testing

Extensive tests were performed on the engineering test unit to prove the design satisfactory prior to prototype packaging design. These tests covered the unit's timing accuracy, actual squib firing capability, and the effects of temperature and voltage changes on its performance.

Temperature tests were conducted on the unit in a temperature chamber over the range of $-70^{\circ}C$ to $100^{\circ}C$. No problems were found at high temperatures but several presented themselves as the temperature was lowered. The output amplifier voltage started dropping off at $-25^{\circ}C$ and squib firing became marginal. Resistor values in the transistor output circuit were changed to provide more base drive and correct the problem.

It was also discovered that the decoder/driver output characteristics change with low temperature and units from different manufacturers change by different amounts. Those obtained from National Semiconductor worked over the temperature range

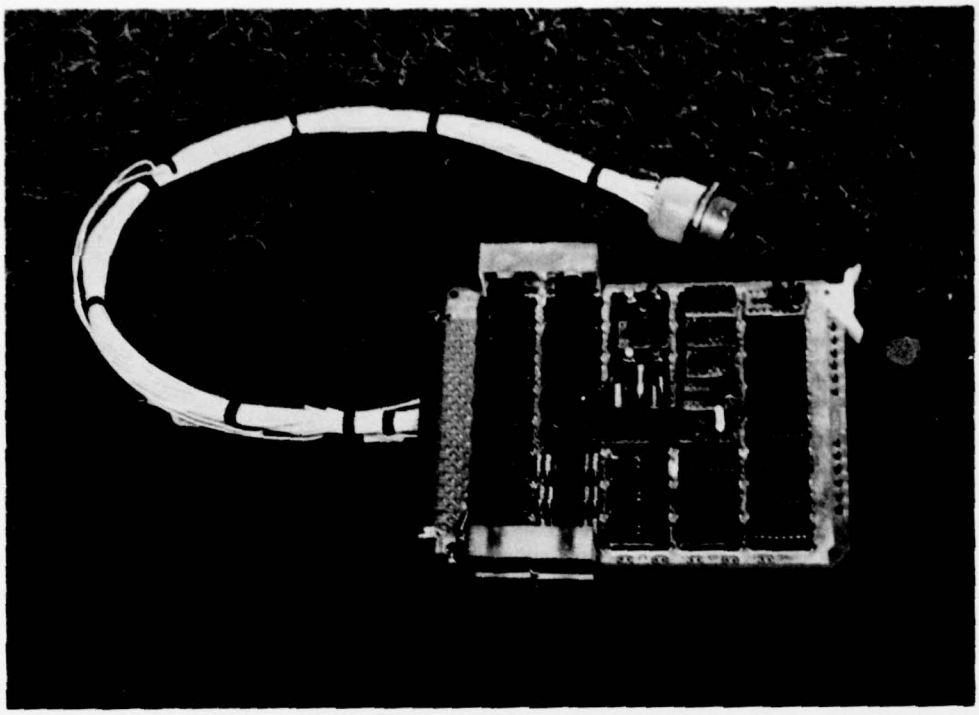


Figure 3-3. Engineering Test Unit

while those from several other manufacturers would not. Thus National's devices are the only ones being used.

Temperature compensation circuitry developed for the current sense circuit, discussed previously, was also tested thoroughly in the chamber.

Voltage tests were conducted over the required operating range of 20 to 30 volts dc and operation of the unit was satisfactory. Two voltage regulators designed into the unit supply 5 Vdc and 18 Vdc to the logic and amplifier circuits respectively. The 18 volt regulator will maintain 18 volts as long as the input remains above 19.5 Vdc. Since the minimum supply voltage to the switch is specified as 20 Vdc no voltage problem will occur in the unit.

All circuit timing within the switch is controlled by a single IC oscillator. The frequency drift of this oscillator was monitored over the temperature range of $-55^{o}C$ to $75^{o}C$. The drift was so small that switch timing stayed within the specification limits.

During the testing a number of live squibs were fired with the switch. In the first live squib test, two squibs were seen as "shorts" by the switch and were skipped over in the firing sequence. They were later measured and found to have a resistance of 0.8 hms. The engineering test unig of the switch was adjusted at that time to sense 0.9 ohms as a short. It was subsequently changed to .7 ohms and the squibs were all successfully fired. The oscillograph recordings presented in Figure 3-4 show the ac firing pulse applied in sequence to four squibs which were located in rocket positions 1, 9, 10, and 19. The increase in amplitude of the ac signal occurs as the squib fires and open-circuits.

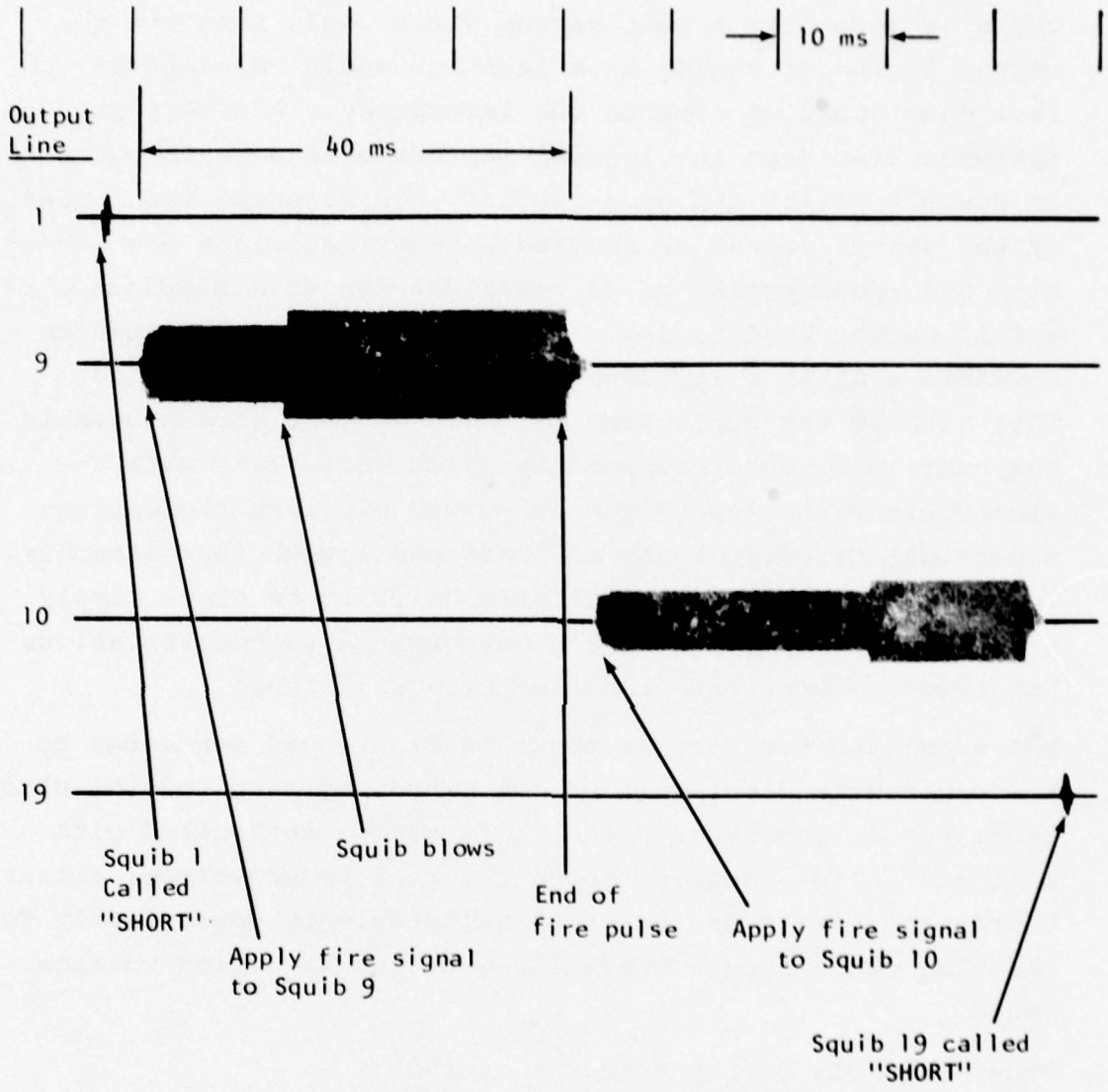


Figure 3-4. Oscillograph Recording of Live Squib Firing

As soon as breadboarding of the electronic switch began, it could be seen that a test set-up which would simulate the actual firing of squibs in a launcher would be necessary to save many hours of time in the laboratory. A simple one-Ohm resistor simulates the initial impedance of a squib but since it doesn't "fire" and open-circuit, the scanning techniques of the switch cannot be checked without laborious disconnecting and reconnecting of 19 resistors for each simulation of a full rocket load firing. Thus a circuit was designed to simulate a squib's impedance and firing characteristics. This circuit was duplicated 19 times and all were housed in box containing other components which would mate with the electronic switch connector and would simulate the entire electrical circuit of the aircraft and launch tube assembly. In addition, timing circuits were built in to check simply and reliably for the switch's conformance to specifications for time-to-first-fire and time-between-firings.

The completed test set is shown in Figure 3-4 connected to the engineering test unit of the switch by means of the black cable and ms connector. The white cable, terminated with alligator clips, connect to an external power source; either battery for field operation or adjustable dc power supply for checking the switch's operation over the specified voltage range.

Other controls on the test set include:

a. Power-on switch and indicator lamp. A replaceable fuze is provided in the power line.
b. Trigger Switch. This switch simulates the pilot's trigger switch in the aircraft and initiates action of the solid state switch.
c. Burst Select Switch. This switch selects one of three time durations for which the trigger pulse is applied to the switch in order to check the following:

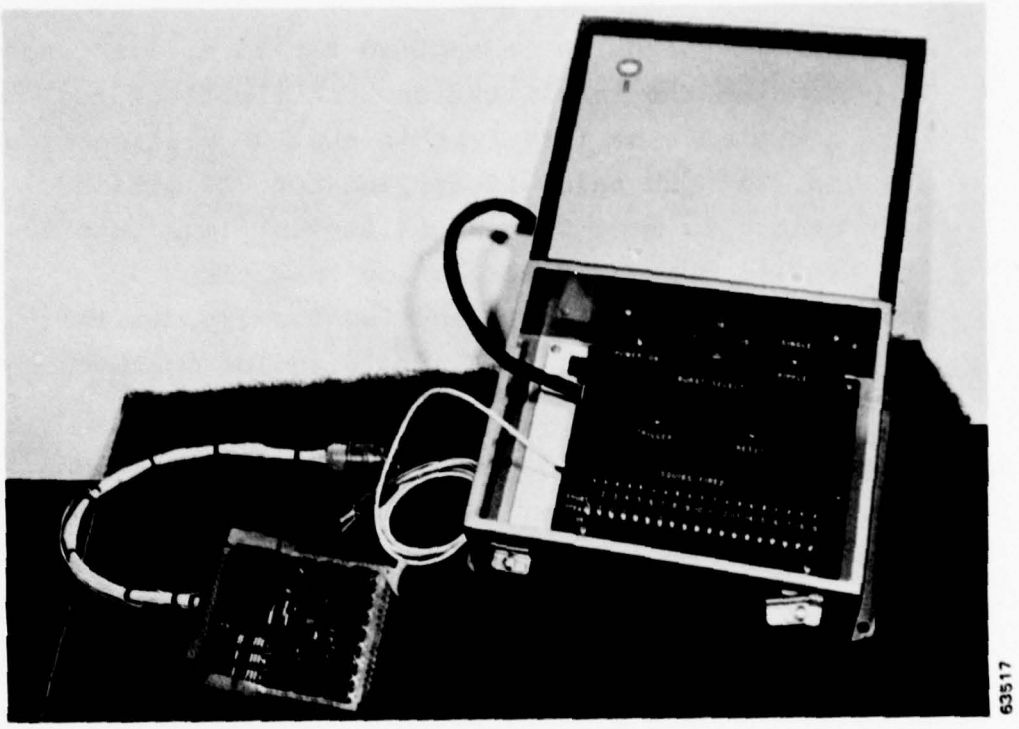


Figure 3-5. Test Set with Engineering Test Unit Attached for Testing

(1) On "1" the pulse is applied for 30 milliseconds. To meet the specification, the first unfired squib must be fired within that 30 milliseconds.

(2) On "18" the pulse is applied for 720 milliseconds. To meet the specification, less than 19 squibs must be fired during that time.

(3) On "19" the pulse is applied for 885 milliseconds and in that time all 19 squibs must be fired.

d. Single/Ripple switch. This switch simulates the single/ripple switch on the launcher and selects the firing mode for the solid state switch.

e. Reset Switch. This switch resets all of the squib simulation circuits back to their "unfired" condition.

f. "Squibs Fired" Indication Lamps. These lamps light to give an indication of which squibs, 1 through 19, have been fired.

g. Squib condition switches. One switch for each of the 19 squibs allows the selection of an open circuit, short circuit, or good squib simulation on that output line from the switch.

Since the squib simulation circuitry requires that a sure-fire current has been applied for more than 10 milliseconds, as called for in the specification, before open-circuiting, all functional requirements of the switch are tested easily and quickly with no additional instrumentation required and no operator skills required. A simple sequence of operating switches and watching for proper lights to light will check out a switch for proper functioning to specifications within a minute or so.

Details of the tester, including circuit diagram, are included in Appendix A.

3.2 PROTOTYPE DESIGN

Design of the prototype switch, of which five units were to be built and delivered under this contract, was undertaken following the successful testing of the engineering test unit. Steps in this design were as follows:

3.2.1 Selection of Components

Since all components used in the engineering test unit were standard items, the same components were selected for use in the prototypes. Military temperature range versions were purchased where they were available within the time frame required. Exceptions were the voltage regulators and output amplifier transistors which are commercial units.

The possible use of hybrid circuits had been considered throughout the circuit design phase of the contract. The originally proposed circuits would not have fit into a package the size of the present mechanical switch without conversion to hybrids.

As circuit design progressed, however, the circuits grew simpler, with fewer components, and it began to look feasible to build the switch of standard components and primary efforts were put toward that goal.

In a lesser parallel effort discussions were conducted with several manufacturers of hybrid circuits and cost estimates were obtained for the tasks involved in converting our circuit to a hybrid. As prototype package design progressed it became clear that the circuit of standard components could be squeezed into the required package but with difficulty and tight tolerances. It became evident that a hybrid circuit would make a unit that would be much easier to produce on a high volume production line. Thus a hybrid design program was undertaken to prove the feasibility of the conversion to a

hybrid and to generate a budgetary cost estimate for the high volume hybrids.

The results of the program, which do prove the feasibility, are presented in Appendix B. Included is a reliability study of the proposed hybrid circuit.

Although feasible, the contract schedule and funds dictated that the five prototypes be built using standard components rather than converting to hybrids.

3.2.2 Package Design

Packaging of the early electronic circuitry into the same envelope as the electromechanical switch appeared to present no problem. This circuitry, operating at 1 MHz, used 19 output transformers wound on ferrite cores of .375 inch OD and .125 inch thick. All 19 would fit in a single row along the axis of the switch.

When the operating frequency was reduced to 10 kHz, however, packaging became very difficult. This lower frequency required an increase in transformer core size to .312 inch OD by .250 inch thick. The 19 transformers would no longer fit in a single row and required one printed wiring board just for them and their associated coupling capacitors.

The final package design consists of two printed wiring boards, a connector, a load/arm switch, and the interconnecting wires for these components. The main printed wiring board contains the logic, current sense, and output amplifier circuits and the voltage regulators. The other, smaller board contains the output transformers and coupling capacitors. These components and their assembly can all be seen in photographs presented in Section 6.

The two boards, switch, connector, and interconnecting wires are molded into a single, solid epoxy unit. Location of the

connector, switch, and 3 mounting lugs are identical to the present electromechanical unit.

3.2.3 Printed Wiring Boards

The prototype boards are of conventional double-sided design with plated-through holes for circuit interconnects. They are made of rigid glass epoxy and the conductive paths have been tinned for protection and ease in soldering.

For a production version, it is suggested that the two boards be combined during the component insertion and soldering steps, as outlined in Section 6, to take full advantage of wave soldering techniques.

3.2.4 Interconnecting Wiring

For the prototype switches, individual point-to-point wiring was used. Flexible circuits and flat cables were considered and estimates were obtained from vendors for their possible use but because of high first-cost and long delivery times they were not used. They are recommended, however, for the final production version of the switch due to the reduction in assembly labor possible and the reduction in wiring errors.

3.3 PROTOTYPE FABRICATION

The five prototype solid-state switches were fabricated in the Ordnance Engineering Division's Experimental Electrical Shop. Fabrication was done by an electronics technician of average skill. Steps in the fabrication can be related to the production line specified in Section 6 and depicted in Figure 6-6 as follows:

a. Component Insertion -- In the prototype fabrication all components were inserted into the printed wiring boards individually and by hand. On the assembly line a number of them are prepackaged on reels and would be inserted by machine.

b. Soldering, Lead Trimming and Cleaning -- For the prototypes, all solder connections between the components and the printed wiring boards were made individually by hand. On the assembly line all connections would be soldered at once on a wave soldering machine. Lead trimming and cleaning would also be completely automatic.

c. Board Handling and Hardware Insertion -- No board separation was required with the prototypes but stand-off insertion was identical to the same procedure in the production line.

d. Board Test -- Since no automated tester is available for testing the individual boards, no test was performed on the prototypes at this stage.

e. Hand Soldering -- Except for automatic wire cutting and stripping, this operation on the prototype switches was almost the same as would be performed on the assembly line. The wires are individually hand soldered between the printed wiring boards, connector, and switch.

f. Assembly -- This operation of fastening the two boards together was identical with the assembly line operation proposed.

g. Test -- Functional testing and troubleshooting of bad units was done in basically the same way that it would be done on the production line. The automatic tester described in paragraph 3.1.3 was used for this test and a similar unit would be designed for the production line. It allows an unskilled operator to quickly and reliably check the completed solid state switch for proper operation. Timing, proper sequencing, proper squib current for firing, and the ability to skip opens and shorts are all checked automatically with a "go/no-go" indication to the operator.

Units that failed the functional test were given to an electronics technician to be analyzed with the normal troubleshooting equipment such as an oscilloscope, digital voltmeter, and logic analyzer.

h. Pot -- Functionally good units were then potted in exactly the same way they would be done on the assembly line except that multiple molds would be used to meet the required production rate. The units were positioned in the mold with the connector and switch firmly held in place. The potting compound was mixed and poured into the mold. When cured, the completed unit was removed from the mold.

i. Test -- A final functional test, identical to that performed before potting, was then run again to insure that potting had not affected any of the switch's characteristics.

3.4 PROTOTYPE TESTING

Each of the five prototype units, three potted and two unpotted, underwent extensive testing of their functional characteristics. Using the automatic tester, proper timing and squib firing sequence were monitored in both the ripple and single-fire modes. The switch's bypass capabilities for both shorts and opens were checked on each output line.

These tests were repeated for each of the five prototypes at temperatures of -55°C, -25°C, 0°C, 25°C, 50°C and 75°C. All functions operated properly over the temperature range with the exception of the short bypass. In three units, sensing a short at -55°C is marginal and the unit will attempt to fire the shorted squib prior to stepping to the next output. This failure is attributed to the decoder/drivers and their inability to sink enough current at low temperature to indicate a short to the current sense detector.

Since the engineering test unit and two of the prototypes do work properly at -55°C, it is felt that all units could be made to work with proper selection of decoder/drivers with high current sinking capabilities. The economics of such a selection would have to be discussed with the manufacturer of the devices prior to the commitment of their use in the high volume production of the switch.

Two of the prototypes were used to conduct firing tests with live squibs. One unpotted unit was used to ripple-fire four live squibs located at output positions 1, 9, 10, and 19. The test was repeated with the switch at -45°C. Both firings were successful in all respects. Oscillograph recordings confirmed proper sequencing and timing.

One potted unit was then used to ripple-fire all 19 squibs. All squibs fired successfully.

All five prototypes were then tested according to the contract to determine conformance to MIS-23156, Paragraphs 4.4.1, 4.4.2, 4.4.3 and 4.4.4.6, as modified by Modification P00005 to the contract. These tests were performed for both FMC and government inspectors.

In general, the test results were considered very successful except for those measured under paragraph 4.4.1.2. In this test the switch is sequenced through all 19 positions and at each position all unfired pins are checked for the presence of less than 5 millivolts. At the start of the test, with only the first output fired, about 80% of the remaining outputs are under the 5 millivolt limit. Several range from 5 to 7 millivolts. As additional lines are "fired" and opened, the noise level on the remaining unfired lines increases until finally all unfired lines are over the 5 millivolt limit. It appears that each line opening adds about 0.5 millivolt to each of the remaining lines and a maximum level of 15 millivolts or so can be obtained under the right combination of conditions.

Time did not permit investigation into solutions to this problem but it is felt that the following would have considerable influence:

a. Output wires between the printed wiring board and the connector, which are presently laced in a tight bundle, should be separated as far as possible and perhaps replaced by shielded conductors to reduce cross-coupling of noise between them.

b. Placement of magnetic shielding material between the output transformers should reduce any coupling that may exist between them.

This induced voltage, at a maximum, is still less than one-tenth of the maximum no-fire voltage (MNFV) allowed for the

Mark I squib and is seen by the squib for only the few milliseconds that other squibs are being fired. The MNFV of 200 millivolts can be applied continuously for 5 minutes without initiation of the squib, according to specification. Thus, the specification for the present intervalometer may be tighter than necessary in this area.

Data sheets recorded by the inspectors covering all of these tests for all five prototypes are being submitted with the hardware.

3.5 TOLERANCE STUDY

Two portions of the circuitry for the solid state switch are based upon analog operation and must be designed to operate within specifications over the temperature range and over the tolerance range selected for the components. These two portions are clock timing and squib resistance detector.

3.5.1 Clock Timing Tolerance

The clock circuit provides the basic timing for the solid state switch. It's output is an ac signal whose frequency, through divide-by-N counters, determines the power output frequency, the fire pulse duration, ripple timing, and the squib scan speed.

This clock circuit consists basically of the SE555V integrated circuit timer, 2 precision resistors and one precision capacitor. Timing accuracy depends on the part tolerance, temperature coefficient, and drift of each component. These factors for the 4 components are listed in Table 3-1.

The specification for ripple timing calls for 35 milliseconds minimum to 45 milliseconds maximum between stations, or 40 ± 5 ms.

An analysis of the variation in frequency due to the variables of Table 3-1 and the temperature range of $-55^{o}C$ to $+80^{o}C$ (when the 4 components are in their circuit configuration as an astable multivibrator) is summarized in Table 3-2. This analysis shows that the clock circuit will provide a stable time base and stay well within the specification

3.5.2 Squib Resistance Detector

In the solid-state switch, the squib resistance detector (current sense circuitry) determines whether or not a good squib is present on the selected output line and signals the

TABLE 3-1

Timing Circuit Variables

Component	Part Tolerance	Temperature Coefficient	Drift
Timer, SE555V			
Timing accuracy	±2%	±100 ppm/°C	
Resistor, 2K	±1%	±100 ppm/°C	
Resistor, 51.1K	±1%	"	
Capacitor, 100 pF	±2%	0 to +70 ppm/°C	±(.05% +.1 pF)

TABLE 3-2

Maximum Timing Circuit Variations

Temperature	Variation MS	Specification, MS
-55°C	37.4 to 43.04	35 to 45
+25°C	38.06 to 42.06	35 to 45
+80°C	37.5 to 42.5	35 to 45

logic to either fire the squib or continue to search for an acceptable squib. This detector is a "window" type, bypassing any resistance lower than the window (i.e., shorts) or higher than the window (i.e., opens). The resistance for an acceptable squib and its wiring to the switch can vary from about 0.7 ohm to 2.4 ohms. Thus, the "window" should be set to call any resistance within that range a good squib.

This detector circuit was simulated on a timeshare computer using models for the diode and transistors of the circuit. While the computer will provide a solution, the validity of the solution depends on a true and realistic representation of the circuit and its elements, especially of the diodes and transistors. Actually two circuits were simulated. One, the dc current level detector to determine the switching points when a load resistor, representing the reflected resistance of the squib, was varied. The other simulated the output circuitry consisting of the coupling capacitor, transformer, and squib. This output circuit simulation was necessary to correlate the squib resistance to output current to determine the values of squib resistance of the window, i.e., the upper and lower switching points of the current detector.

Many simulations of the current level detector were tried. The final simulation used latches controlled by the voltage across diode junctions to simulate transistors. The junction voltages were determined by actual measurement of the transistor base-emitter junctions.

Both upper and lower limits of the resistance window at three different temperatures were determined through computer simulation. The three temperatures correspond to the operating environment of the solid state switch, i.e., $-55^{o}C$, $25^{o}C$ and $80^{o}C$.

The results were:

	SQUIB RESISTANCE (ohms)		
"Window" limit	-55°C	+25°C	80°C
Upper	2.0	2.3	2.5
Lower	.55	.63	.71

These results indicate that the squib resistance detector can determine acceptable squibs but the variations with temperature fall slightly outside of the desired range.

Since the computer solution is dependent on the validity of the models used, the variations indicate that further simulation with more accurate model parameters, determined from actual testing of the semiconductor devices, is necessary.

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SECTION 4
RELIABILITY ANALYSIS

A reliability analysis was undertaken of the static switch design to establish a predicted value of Mean Time Between Failures (MTBF) for the unit. The analysis included a worst-case stress analysis of the circuitry, evaluation of the quality level of parts used, and a compilation of predicted failure rates.

Based on available information relating to the quality level of the purchased electronic parts, the following is a summary of the predicted MTBF for the static switch. The three values shown reflect different screening levels and testing which can be performed on the integrated circuits.

IC Qual. Level	MTBF
Commercial	5,187 hours
MIL-M-38510, Class C	23,733
Vendor Equiv., 883B	28,257

4.1 CIRCUIT STRESS ANALYSIS

A worst-case stress analysis of all electronic components was performed utilizing logic diagram SKAM 8175 as the basic circuit schematic. In general, stresses were computed based on conservative approximations of voltage and current levels applied, such that in most cases the computed stress levels are probably higher than will be experienced in actual operation. Even so, with few exceptions stress ratios (i.e. the ratio of actual to rated electrical stress) were found to be consistently low, with approximately 75% of the components experiencing stress of 25% or less of rated major electrical parameter value.

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4.2 RELIABILITY PREDICTION

The predicted values of failure rates are based on the data and methods of MIL-HDBK-217B. In determining the value of the various multipliers, the following assumptions were made.

a. The environment was considered to be "Aircraft, Uninhabited Area" in determining the environmental multiplier, π_E.

b. Maximum temperature was assumed to be +71°C, based on the requirement for testing to MIL-STD-810, Method 501, Procedure I.

c. Failure rate levels for the established reliability (ER) parts were assumed as level R for resistors and level M for capacitors.

d. The 2N2907 and 2N2222 transistors were considered as JAN devices, while the 1N4001 diode and the 2N4918 and 2N4921 transistors were assumed to be commercial quality level.

e. Integrated circuits were assumed to be military temperature range, but of commercial quality. However, additional computations were made considering IC's to be MIL-M-38510, Class C quality, and also for screening to MIL-STD-883, Class B.

f. Cycling rates for the connector and the Load/Arm switch were assumed as less than 40 cycles/1000 hours.

g. The temperature rating of the transformer insulation was assumed to be 85°C.

Based on the above assumptions, the circuit Stress Analysis sheets presented in Appendix C, list the predicted failure rates for each component in the static switch. An MTBF value may be calculated by taking the reciprocal of the summation of the individual failure rates:

$$MTBF = \frac{1}{\Sigma FR} \qquad \frac{1}{192.791X10^{-6}}$$

$$= 5,187 \text{ hours}$$

It should be noted that this figure is merely the predicted mean time between random failures of individual components; it does not necessarily imply that the switch will fail to function properly, or at least adequately, after that number of hours. Since a failure mode and effects analysis was not a part of this effort, it is unknown what the effect on system performance is for failure of each part. It is likely, however, that failure of some parts due to drift of some parameters out of tolerance, would not always preclude adequate output. Nevertheless, the MTBF value does give a relative picture of the switch reliability.

The major contributors to the total failure rate are seen to be the integrated circuits, which account for about 87% of the summed value.

This is due largely to the assumption of commercial quality, resulting in a quality level multiplier of 150 for these devices. If the IC's are purchased to the requirements of MIL-M-38510, Class C, this value drops to 16, resulting in an increase in MTBF to 23,733 hours. Further, since the specification, par. 3.7, calls for testing of all microelectronic devices to MIL-STD-883 by the contractor or a subcontractor, it may be logically assumed that the IC's will be screened at least to the vendor equivalent of MIL-STD-883, Class B. In this case, the quality level multiplier may be further reduced to a value of 10, resulting in an MTBF value of 28,257 hours.

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4.3 OPERATING CYCLES

It is recognized that the system operating hours, that is, the total time during which the circuit is energized, is not the parameter of major interest. Rather, since the unit is essentially an intermittently pulse-operated switch, the number of firing cycles is a more useful indicator of unit reliability. Since the circuit is energized only when the trigger switch is closed, and since the closure time of this switch may be only a fraction of a second on many closures, a direct translation of operating hours to cycles will probably lead to an unrealistically high number of cycles between failures (MCBF). Since the circuit will experience considerable capacitive and inductive transients during pulse operation, the stresses on many parts will be greater, in sum, than if the circuit were to be continuously energized. Although the scope of this effort did not allow for system analysis to the depth required for a precise quantitative determination, it is estimated that at least a factor of ten is required to reflect the transient effects mentioned. Knowing the timing of the system, a total time to cycle through all switch positions can be determined and from this value an approximate translation to cycles per operating hour computed.

4.4 RECOMMENDATIONS

a. The variation in the quality level of the integrated circuits depending on screening level used has been discussed above. It is recommended that screening of the IC devices be undertaken to a level equivalent to MIL-STD-883, Class B. This will provide a substantial increase in the predicted values of MTBF and MCBF, and in particular will detect those devices prone to infant mortality.

b. It is further recommended that all capacitors be purchased to ER level R as are the resistors. While this will achieve only a relatively small increase in MTBF, about 5%, it does provide added confidence, and would be consistent with the resistor quality level.

c. One capacitor, C22, acting as a filter at the output of the 18V regulator, is stressed to 90% in voltage. It is recommended that a 50V rated unit replace the current 20V rating.

FMC

SECTION 5
EMI ANALYSIS

5.1 SUSCEPTIBILITY OF THE SQUIB

For reasons of safety and reliability, the current induced through the squib from unwanted external sources must be kept as low as possible. The maximum no-fire current for the Mark I Mod 0 Squib is 200 milliamperes. Normal practice is to limit the current to 10% to 15% of the maximum no fire current. Therefore, maximum current should be limited to 20 to 30 milliamperes.

For this analysis, squib current level will be the criteria. The Mark I Mod 0 sensitivity to RF current has been shown to be the same as its DC sensitivity. Therefore, there will be no safety factor added for the RF currents.

5.2 RADIATION FIELD ENVIRONMENT

The maximum far field electromagnetic radiation environment for electroexplosive devices as required by the three services (Army, Air Force and Navy) are different. The Army requirement for this analysis was taken from a document, "Electromagnetic Radiation (EMR) Interim Criteria for Missile Systems", received from MICOM with a letter dated 11/19/75. The Air Force requirement was determined from sections of MIL-STD-1512 and AFSC Design Handbook DH2-5. The Navy's requirement is contained in MIL-STD-1385. These requirements are summarized in Table 5-1.

Since the launchers are to be used by all three services, the requirements were consolidated into one table. The consolidated requirements are shown in Table 5-2 at the frequencies of interest.

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TABLE 5-1. ELECTROMAGNETIC FIELD CRITERIA

Service	Frequency (MHz)	Average Power Density (Watts/Meter^2)
Army	0.1 - 100	26.5
	100 - 12,400	106
Air Force		
	.03 - 40,000	100
Navy		
Communications		
	0.25 - 0.535	239
	2 - 32	26.5
	100 - 156	0.1
	225 - 400	0.1
Radar		
	200 - 1215	100
	1215 - 1365	50
	2700 - 3600	780
	5400 - 5900	1050
	7900 - 8400	1750
	8500 - 10440	1500
	33200 - 40000	40

TABLE 5-2 - POWER DENSITY REQUIREMENT

Frequency (MHz)	Average Power Density (Watts/Meter^2)
.030	100
.100	100
.250	239
.535	239
2	100
32	100
100	106
225	106
1215	106
2700	780
5400	1050
7900	1750
8500	1500
40,000	100

The near field environment is not covered by those documents covering the far field. In order to study this area, an assumption is made. Due to the low impedance involved, the magnetic inductive field is of primary concern. For the induction coupling, the current level in the nearby conductor is assumed to be 25 amperes, and the separation between the launcher and the conductor is assumed to be 40 inches (approximately 1 meter).

5.3 SHIELDING

The launcher skin of aluminum, 40 mils in thickness, provides the shielding for the solid-state switch. However, the skin

should not have any openings. Where openings are necessary, such as for access doors, a covering for the opening should provide low impedance path by use of RF gaskets and conductive surfaces.

5.4 SQUIB CIRCUIT WIRING

The squib circuit wiring is assumed to be similar to a monopole with the squib bridgewire being the load. The length of the AWG 20 wire varies from 11 inches to 34 inches. The spacing between the wire and the return, which is the launcher structure and skin, is assumed to be .125 inch. For this analysis the longest lead (34 inches) will be used. This will provide a lower sensitive frequency when using the monopole antenna concept.

5.5 FAR FIELD ANALYSIS

In the far field region the squib and its associated wiring is assumed to be a monopole with the squib being the load. The squib resistance is 1 Ohm, and the wiring varies in length from 11 inches to 34 inches. We will consider the longer length due to its larger susceptibility within the rocket launcher. It is important for effective shielding that the aluminum skin be continuous without any openings. Being continuous becomes increasingly important at higher frequencies.

The power delivered to the squib is given as,

$$W_R = P_A \times S \times A_E$$

Where W_R = Power available to squib (watts)

P_A = Power density to electromagnetic radiation field ($Watts/_{Meter^2}$)

S = Shielding loss

A_E = Effective aperture of squib wiring (Meter^2)

In order to consider the worst case condition, it is assumed that there is no mismatch between the antenna (the wiring) and the load (the squib). The characteristic impedance of a lead, .032 inch diameter, separated from ground by .125 inch is approximately 164 Ohms. The radiation resistance for a quarter wave monopole is approximately 36 Ohms. In reality then, there is a mismatch, and this assumption will result in a higher calculated squib current than actual.

The gain of the antenna is assumed to vary with frequency. At quarter wave frequency, f_o, to 7 times f_o, the gain is constant. At frequencies below f_o, the gain increases 20 dB per decade. The squib wiring is assumed to be a quarter wave monopole which has a gain of 3.28 above an isotropic antenna. The use of such a high gain will provide a margin of safety. Using the gain, effective aperture area is determined by,

$$A_e \text{ (meter}^2) = G_R \times 3.28 \times \frac{\lambda^2}{4\pi}$$

G_R = Relative antenna gain, varies with frequency

λ = Wavelength, meters

Shielding effectiveness can be defined as the total attenuation of the RF energy in attempting to penetrate a barrier. This shielding loss, in dB, is generally expressed as:

$S(dB) = A + R$

Where A = Absorption loss (dB)

R = Reflection loss (dB)

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The absorption loss, A, is determined by the material, its thickness and the frequency of radiation.

$$A\ (dB) = 3.334 \times 10^{-3}\ t \sqrt{f\sigma\mu}$$

where: t = thickness in mils

f = frequency, in Hz.

σ = relative conductivity, (referred to copper)

μ = relative permeability (referred to free space)

For this squib susceptibility analysis, the aluminum skin of the rocket launcher is assumed to be 40 mils in thickness. For aluminum σ is 0.61 and μ is 1.

The reflection loss, R, is the result from the mismatch of the impedances at the air-to-aluminum interface seen by the electromagnetic wave. This loss was determined using procedures in NAVWEPS OD 30393, and becomes greater as the frequency decreases.

For this analysis, the more significant loss is used in determing susceptibility. That is, at frequencies up to 1 MHz, the reflection loss is used; above 1 MHz, the absorption loss is used. Utilizing these losses the squib current is calculated from;

$$W_R = I_S^2 R \quad ; \quad I_S = \sqrt{\frac{WR}{R}}$$

Where W_R = Power available to squib (watts)

I_S = Squib current (amperes)

R = Resistance of squib (one Ohm for the Mark I Mod O.)

With the shielding effect of the aluminum skin of the launcher taken into consideration, the squib current levels are below the required criteria of 20 to 30 milliamperes maximum. The induced squib currents at the various frequencies are listed in Table 5-3.

TABLE 5-3 INDUCED SQUIB CURRENT

Freq. MHz	Power Density W/M^2	Shielding Loss A dB	Shielding Loss R dB	Relative Antenna Gain dB	Squib Current Ampere
.03	100		121	-70	1.44×10^{-5}
.1	100		116	-59	2.73×10^{-5}
.25	239		112	-51	6.71×10^{-5}
.535	239		108	-42	1.40×10^{-4}
2	100	150		-33	5.43×10^{-7}
32	100	590		-9	5.37×10^{-29}
100	106	1040		0	1.58×10^{-51}
225	106	1560		0	7.01×10^{-78}
1215	106	3600		+6	2.59×10^{-180}
2700	780	5400		+13	7.08×10^{-270}
5400	1050	7650		+19	2.59×10^{-382}
7900	1750	9250		+22	3.23×10^{-462}
8500	1500	9600		+23	9.86×10^{-480}
40000	100	20800		+35	2.15×10^{-1040}

5.6 NEAR FIELD ANALYSIS

In the near field the analysis is directed toward inductive coupling of the squib lead to the magnetic field. The induced voltage is given as,

$$e = 3.19 \times 10^{-8} \; f \; L \; i \; \ln \frac{r_2}{r_1}$$

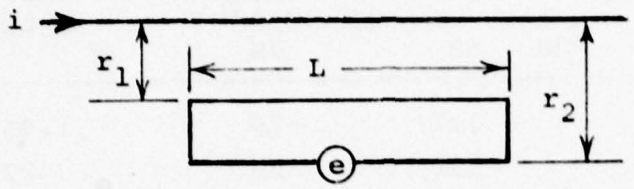
When e = induced voltage (volt)

f = frequency (Hz)

L = length of coupling (inches)

i = current in nearby conductor (ampere)

r_1, r_2 = distances from conductor (inches)



For this analysis, it is assumed that L = 34 inches, r_1 = 40 inches, r_2 = 40.125 inches and i = 25 amperes. Therefore,

$$e = 8.46 \times 10^{-8} \text{ f volts}$$

The far field region is defined as the region whose distance is one wavelength beyond the transmitting antenna. Therefore, the near field will be assumed to be the region within one wavelength. Since we have previously assumed that the distance from the conductor is 40 inches, our analysis will be limited to frequencies whose wavelength is 40 inches or more. The cut-off frequency is approximately 300 MHz. At higher frequencies the region at 40 inches becomes far field, and the far field analysis will hold.

Due to the aluminum skin of the launcher whose thickness is 40 mils, there is sufficient attenuation to protect the squibs. The squib currents due to the near field inductive coupling are listed in Table 5-4

TABLE 5-4

Freq. (MHz)	R_h (dB)	I_S (current, ampere)
.030	57	3.59×10^{-6}
.100	62	5.34×10^{-6}
.250	66	1.06×10^{-5}
.535	70	1.43×10^{-5}
2	75	3.01×10^{-5}
32	87	1.21×10^{-4}
100	92	2.13×10^{-4}
225	96	3.02×10^{-4}
300	97	3.59×10^{-4}

In the actual circuit there will be in series with the squib the output transformer's secondary winding. The added impedance of the secondary winding and the transformer leakage inductance will decrease the squib current further. The total of the two inductances has been measured to be approximately 104 microhenries.

5.7 CONCLUSIONS

Based upon the above analysis, it is concluded that the Mark I Mod O squibs are safe from ignition and dudding when shielded by the launcher's conductive outer skin. The far field analysis indicates that the maximum squib current is less than 1% of the maximum no fire current (200 milliamperes). In the near field the maximum squib current is less than 2% of the maximum no fire current. These current values were determined with optimum conditions, and in reality will probably never be encountered.

It is imperative, though, that the enclosing outer skin have minimum number of openings, and these openings should have conductive covers providing a low impedance path to RF by use of highly conductive gaskets, surfaces and finishes.

References used in the preparation of this analysis are presented in Appendix D.

5.8 EMI TESTING

To obtain some verification of the above analysis, one of the prototype solid-state switches was subjected to EMI testing at a subcontractor's test facility. The unit was mounted in a rocket launcher along with one inert rocket with a one ohm resistor simulating a squib inserted in it.

A transducer to monitor actual squib current induced by a radiated field was installed near the switch. It's output was brought out to measuring instruments, located outside of the screen room, through a specially made access panel and rigid and flexible metal conduit. Figure 5-1 shows the test set-up with the launcher mounted within the radiating antenna used for susceptibility measurements at frequencies up to 200 megahertz.

Although testing was not quite complete at the time of writing this report, all squib currents measured were well below the no-fire current specified for the squib and thus it is felt that no hazard is presented by use of the solid-state switch. Measurements under several sets of conditions were taken on both the solid-state switch and the electromechanical intervalometer. Squib currents were comparable and in some instances the solid-state switch currents were lower.

Preliminary test data sheets of tests performed to date have been included in Appendix D. The final EMI test report, to be received from the subcontractor within a few weeks, will be forwarded at that time.

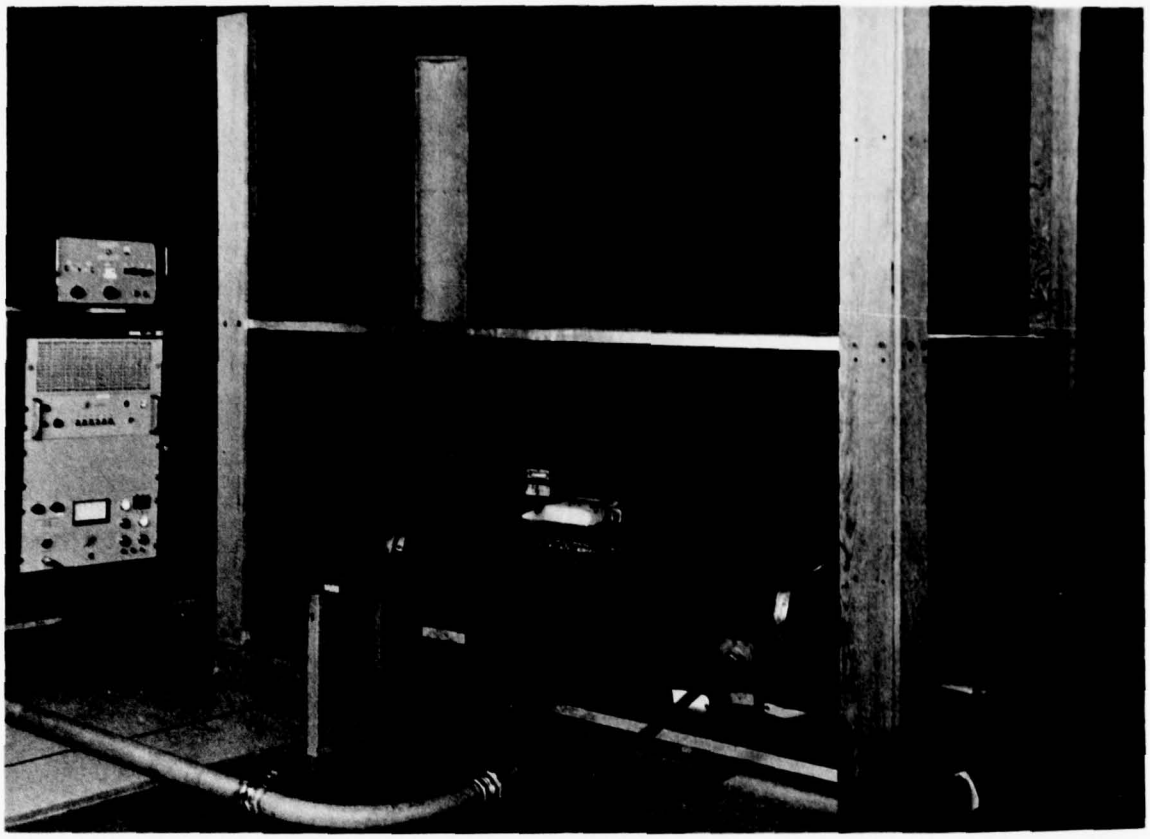


Figure 5-1. EMI Test Setup

FMC

SECTION 6
PRODUCTION LINE DESIGN

A solid-state switch, which sequentially provides the electrical energy to fire nineteen rockets, has been developed as reported in previous sections of this report to replace the existing electromechanical intervalometer. The objective of this part of the report is to establish a production line concept to manufacture one thousand solid state switches per week. To fulfill this objective, lists, photos, drawings and specifications will be provided as required to specify the production line. The production environment and production and test equipment will be identified and test equipment calibration control requirements will be discussed.

6.1 INTERVALOMETER DESIGN

The complete assembled electronic switch is shown in Figure 6-1. Only three features distinguish the completed unit as being anything but a solid block of potting material. A manually operated control knob is provided to arm and dis-arm the unit as required, an electrical connector provides an electrical interface with the rest of the rocket system and three threaded inserts are molded into the body to provide a mounting means.

The unpotted unit, in contrast, looks like and is a collection of integrated and discrete electronic components as shown in Figure 6-2.

6.1.1 PARTS

The completed electronic switch requires a total of 95 electronic parts plus 7 individual pieces of hardware and 48 interconnecting wires.

Fifty-three of the electronic parts, or 57% can be identified as machine insertable into the printed wiring boards. These

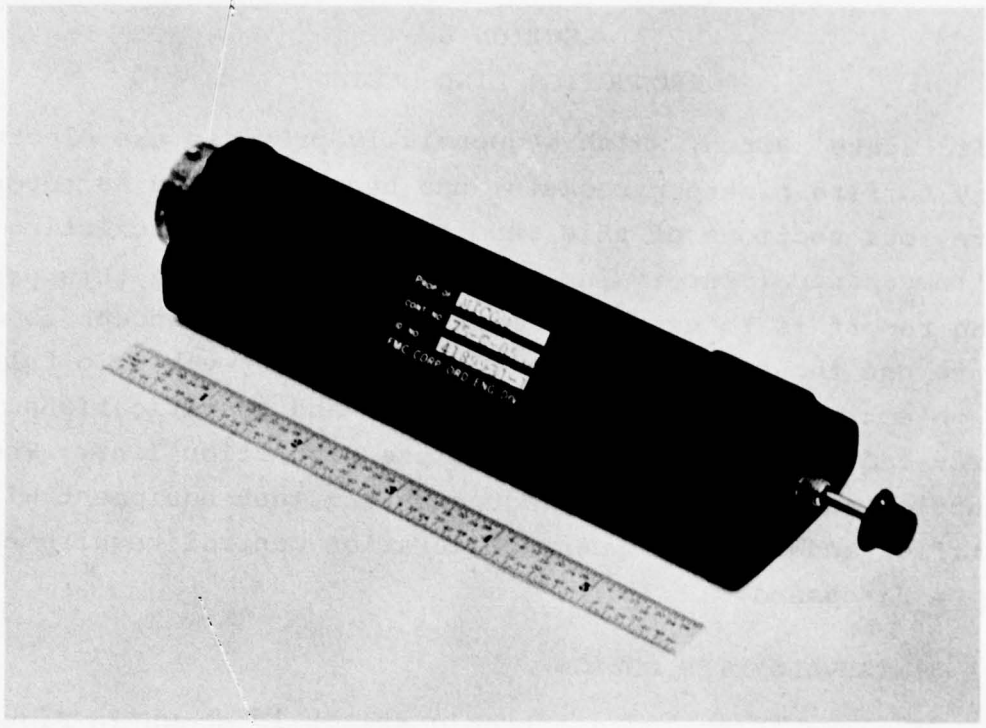


Figure 6-1. Complete Switch Potted

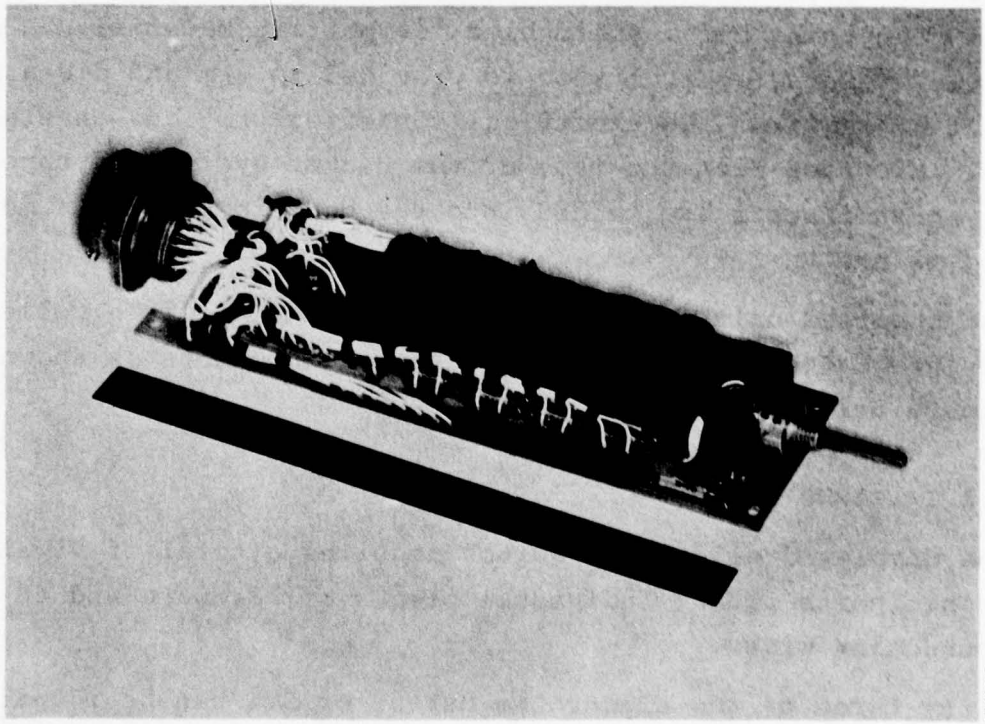


Figure 6-2. Switch Unpotted

are:

24 Axial lead ¼-watt resistors
1 Axial lead diode
(Same physical size as ¼-watt resistor)
19 Axial lead capacitors
(Same physical size as ¼-watt resistor)
5 (16) Terminal DIPs
5 (14) Terminal DIPs

Forty of the electronic parts, or 43% are considered to be machine insertable only at considerable added cost and thus will be inserted by hand. These parts are:

8 Capacitors
6 Transistors (signal)
2 Transistors (power)
1 Thermistor
1 Resistor
2 Regulators
19 Transformers
1 DIP (8 terminal)

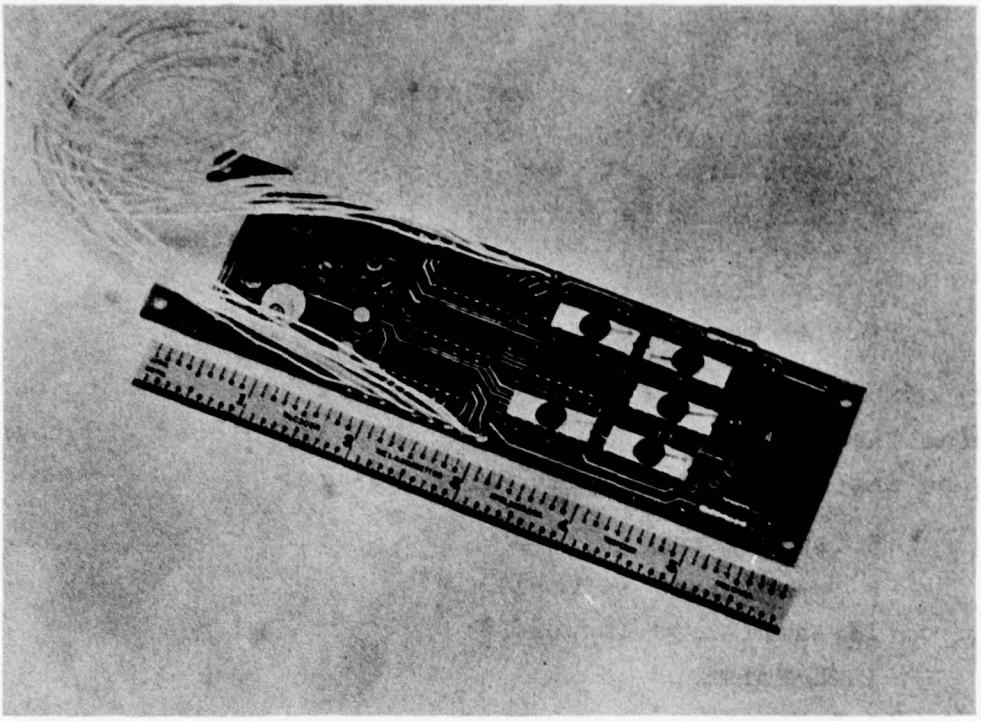
One switch and one connector bring the total number of electronic parts to 95.

6.1.2 BOARDS

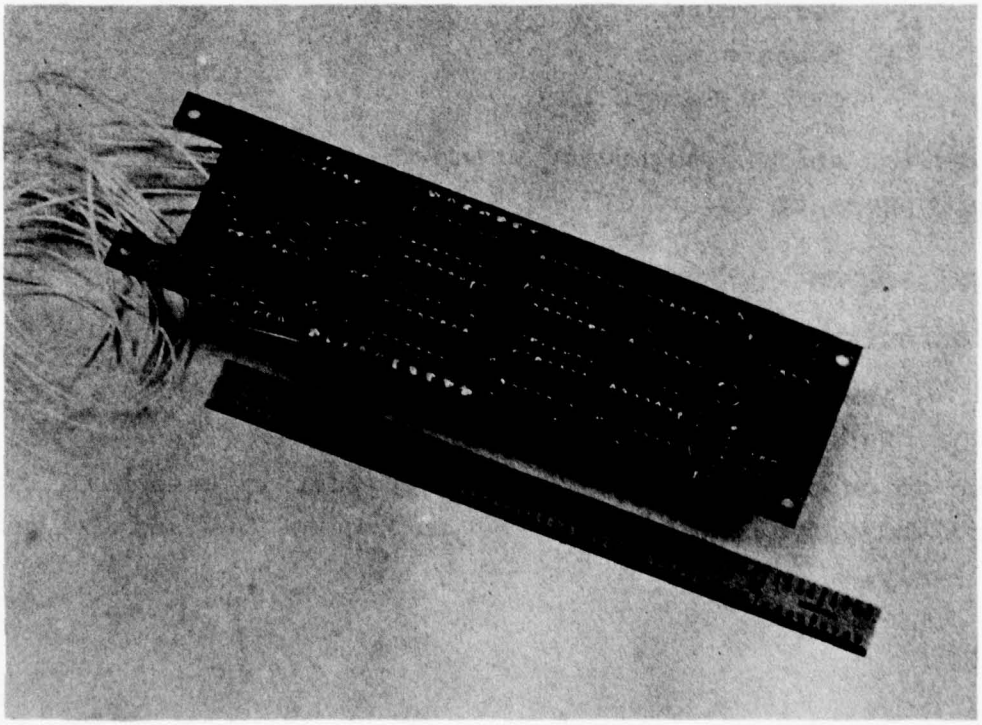
All insertable components go on the logic board except

19 Axial lead capacitors
19 Transformers

which go on the output board. The completely assembled logic board and output board are shown in Figures 6-3 and 6-4 respectively.

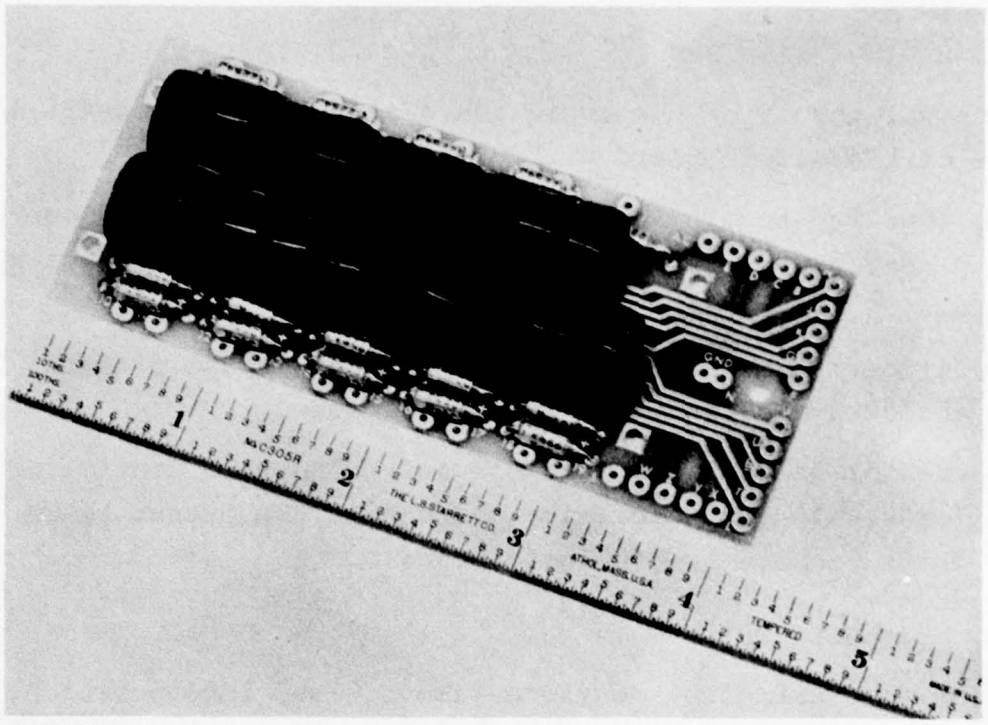


FRONT

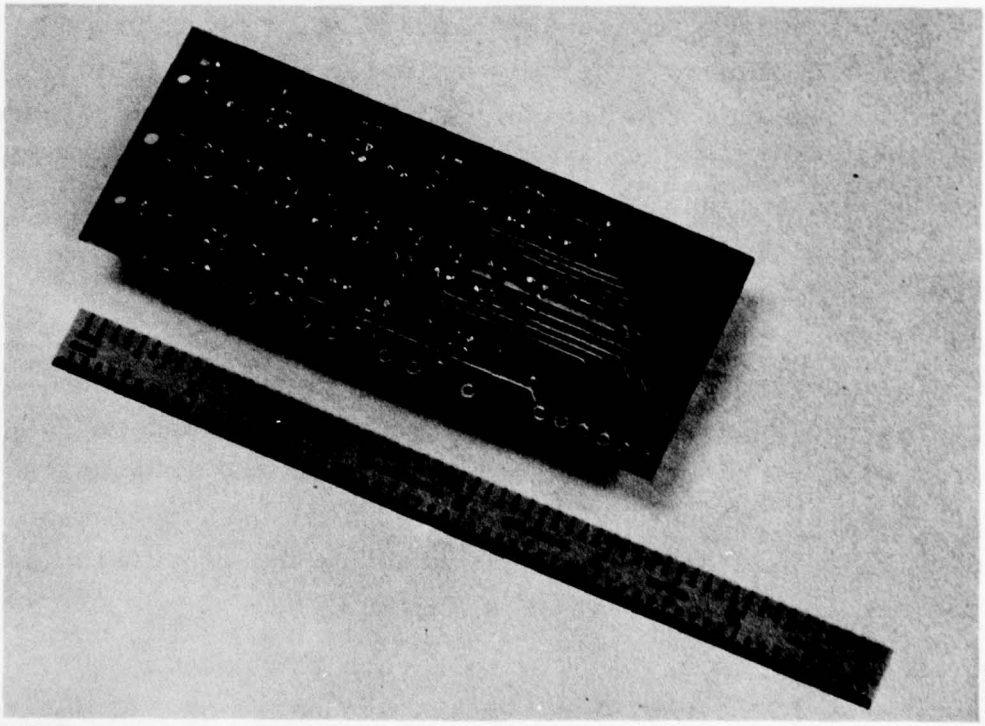


REAR

Figure 6-3. Completed Logic Board



FRONT



REAR

Figure 6-4. Completed Output Board

FMC

6.1.3 WIRING HARNESSES

Terminals 1 thru 9 of the logic board connect to terminals 1 thru 9 of the output board with a single harness.

In the same way terminals 10 thru 19 of the logic board connect to terminals 10 thru 19 of the output board with a single harness.

Two additional wires connect the AC bus and ground of each board together and constitutes a 3rd harness.

The connector is prewired with the fourth harness consisting of 24 leads. 20 of these leads connect to the output board and 4 leads connect to the logic board.

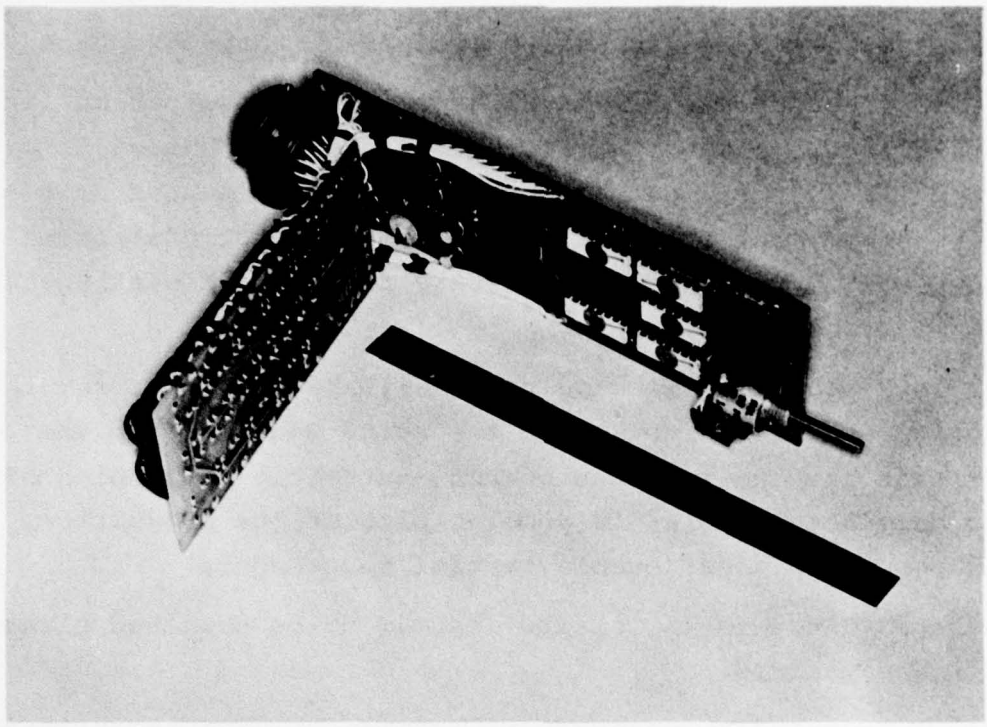
6.1.4 ASSEMBLED UNIT

With the four harnesses mentioned above wired into position, all that remains to complete the assembly is to connect 3 leads from the switch to the logic board and fasten the output and logic boards together mechanically using the two standoffs swaged into the logic board and two screws. Figure 6-5 shows the completed assembly before and after mechanical coupling of the boards.

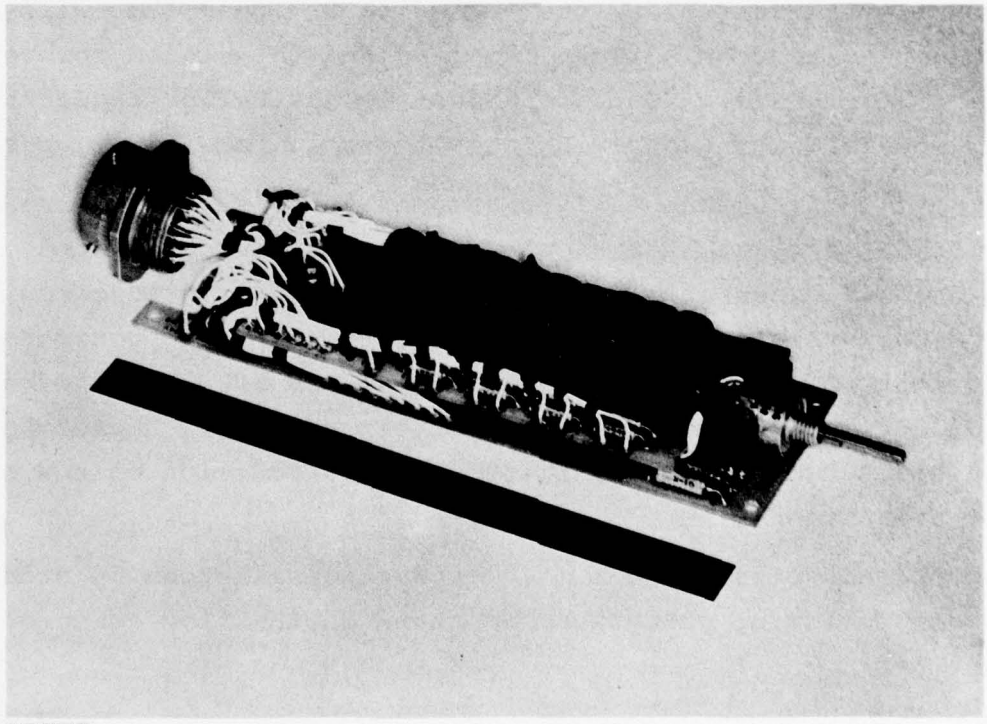
6.2 PRODUCTION LINE SPECIFIED

To produce 1000 solid state switches per week in an essentially serial manner, one switch must appear at the output end of the line at the rate of one every 2.1 minutes, based on 35 hours per week of actual production. Therefore, 1000 units per week will be produced if the duration of each operation, including material handling, that makes up the production line, averages out to 2.1 minutes, as a maximum.

In the allocating of stations within this production line, time estimates for doing manual tasks are based on FMC derived time and motion studies. For tasks involving machine



BEFORE



AFTER

Figure 6-5. Completed Unit Before and After Mechanical Coupling

operations, the vendor's stated production rates are used.

The electrical/electronic parts used in this production line are assumed to be good, having been tested and burned-in by the supplier. Parts can be purchased in this manner at a small premium cost per part. If parts were not pre-tested and burned-in, it would be necessary to add work stations to accomplish this task.

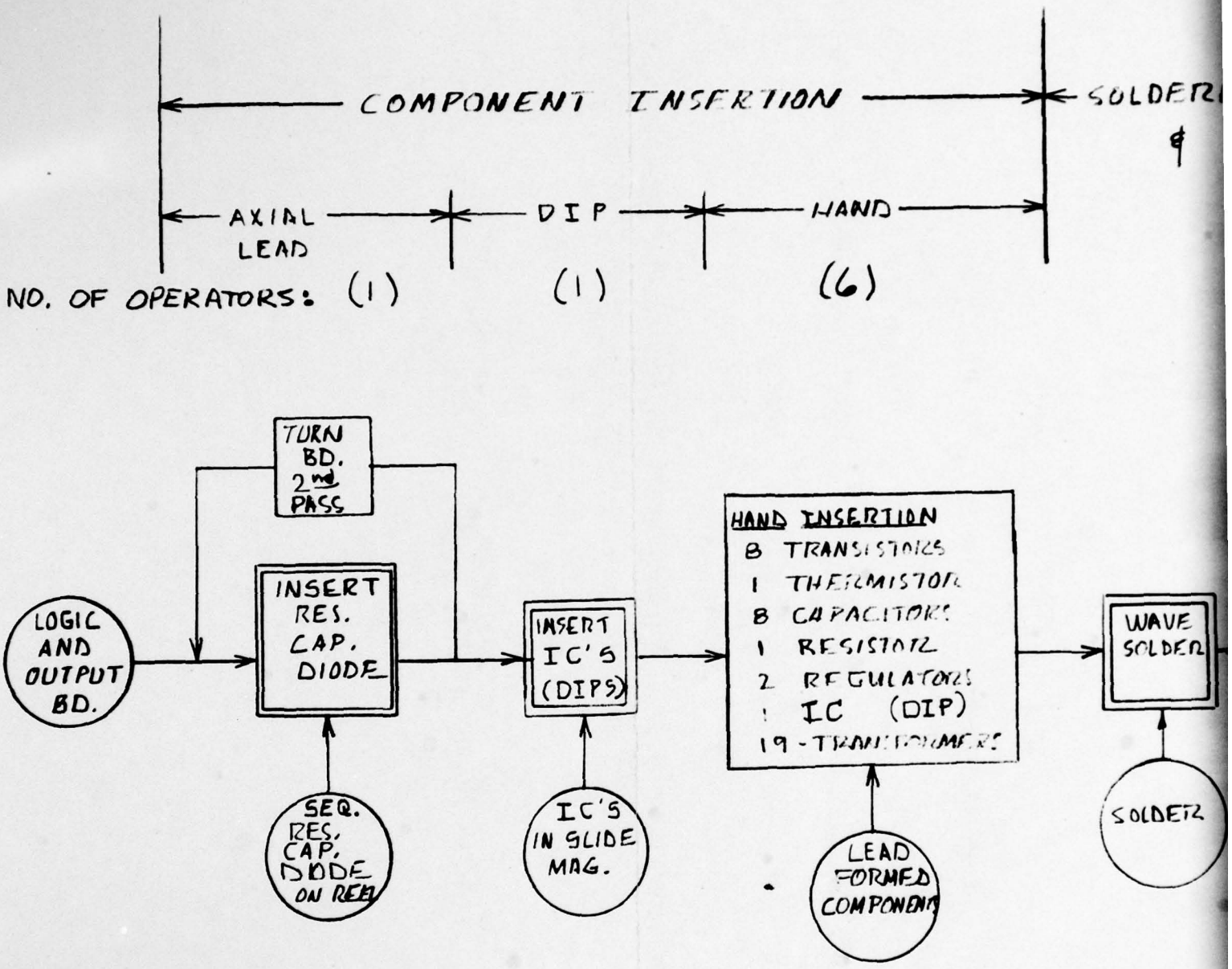
Axial lead, machine inserted parts will be obtained from the vendor taped and on reels with the parts sequenced in the order that they go into the board. Automatic sequencing of parts onto taped reels, if done as part of the production, would require a considerable captial investment.

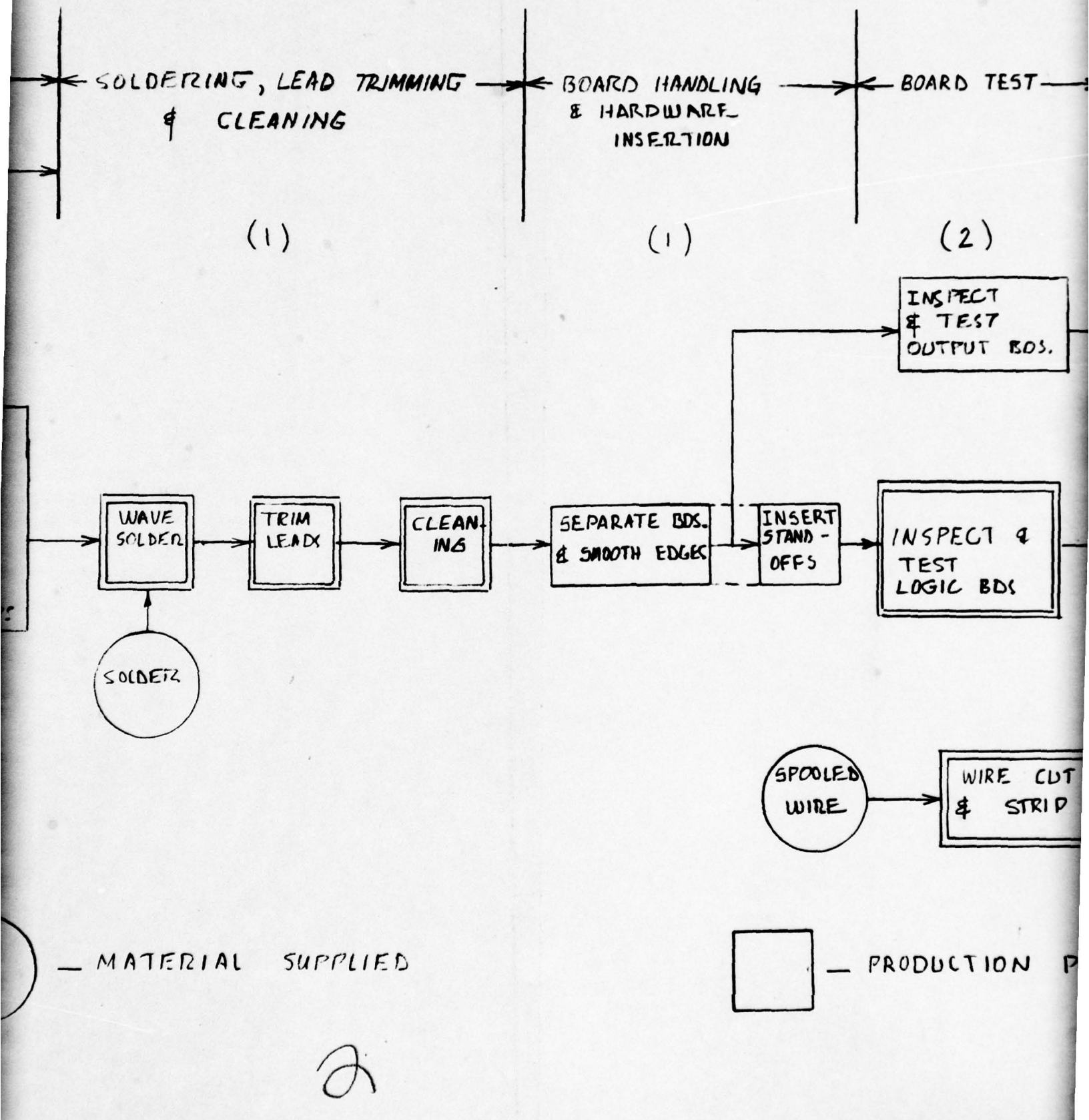
Integrated Circuits (IC's) are assumed to be obtained already in slide magazines.

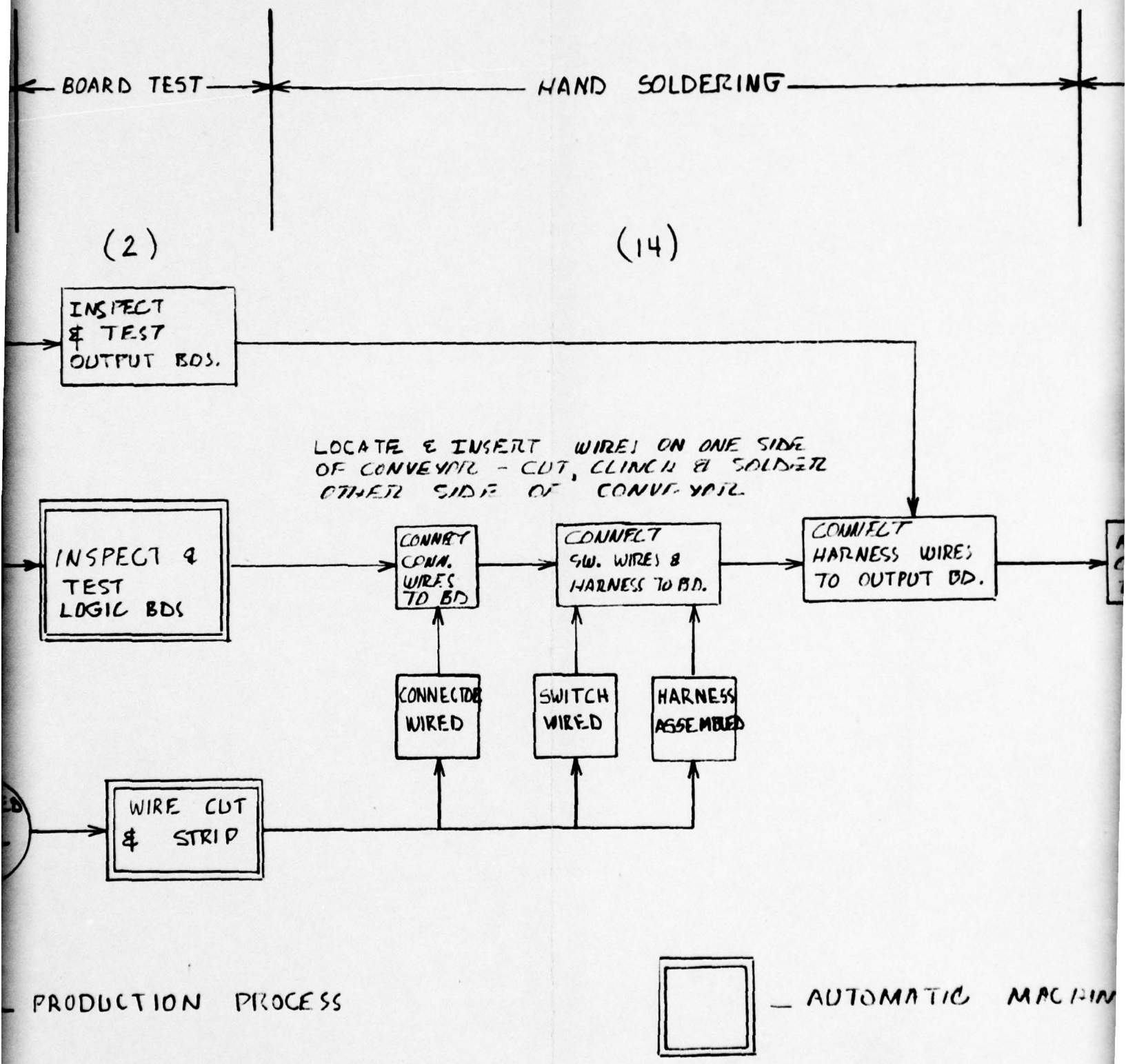
Manually inserted components are assumed to have their leads already cut to length and pre-formed in a manner that will apply spring tension between the lead and the plated through holes of the board. Some companies, such as Heller Industries, Inc., specialize in supplying components in this configuration.

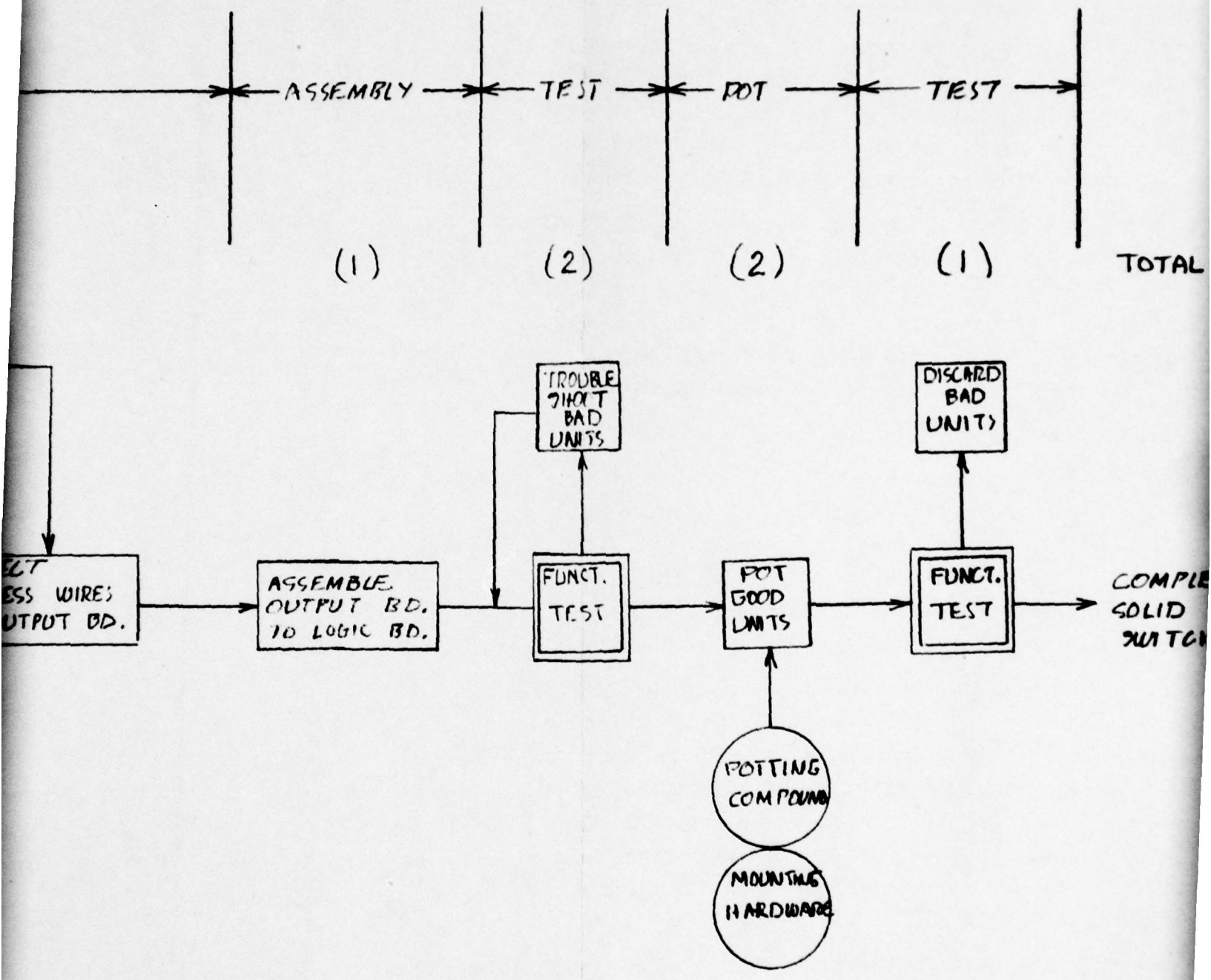
Printed circuit boards will be assumed to be supplied already inspected and tested for shorts, opens and correct plated through hole resistance. The manufacture of printed circuit boards would require a separate production line approximately equivalent to the line proposed. Suppliers of printed circuit boards regularly inspect and test their product. Therefore, it should not be necessary to repeat this function on the proposed production line.

The proposed solid state switch production line can be ordered into the following processes, as shown in the flow graph of Figure 6-6:


COMPONENT INSERTION
SOLDER
AXIAL LEAD
DIP
HAND
NO. OF OPERATORS: (1) (1) (6)
TURN BD. 2nd PASS
LOGIC AND OUTPUT BD.
INSERT RES. CAP. DIODE
INSERT IC'S (DIPS)
HAND INSERTION
8 TRANSISTORS
1 THERMISTOR
8 CAPACITORS
1 RESISTOR
2 REGULATORS
1 IC (DIP)
19 - TRANSFORMERS
WAVE SOLDER
SEQ. RES. CAP. DIODE ON REEL
IC'S IN SLIDE MAG.
LEAD FORMED COMPONENTS
SOLDER
LEGEND:
MATER

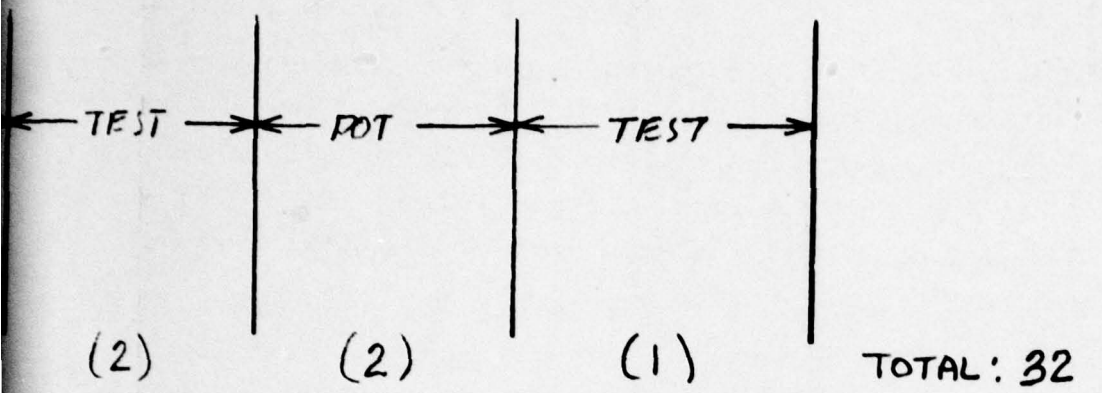

SOLDERING, LEAD TRIMMING & CLEANING
BOARD HANDLING & HARDWARE INSERTION
BOARD TEST
(1)
(1)
(2)
INSPECT & TEST OUTPUT BDS.
WAVE SOLDER
TRIM LEADS
CLEAN-ING
SEPARATE BDS. & SMOOTH EDGES
INSERT STAND-OFFS
INSPECT & TEST LOGIC BDS
SOLDER
SPOOLED WIRE
WIRE CUT & STRIP
— MATERIAL SUPPLIED
— PRODUCTION P

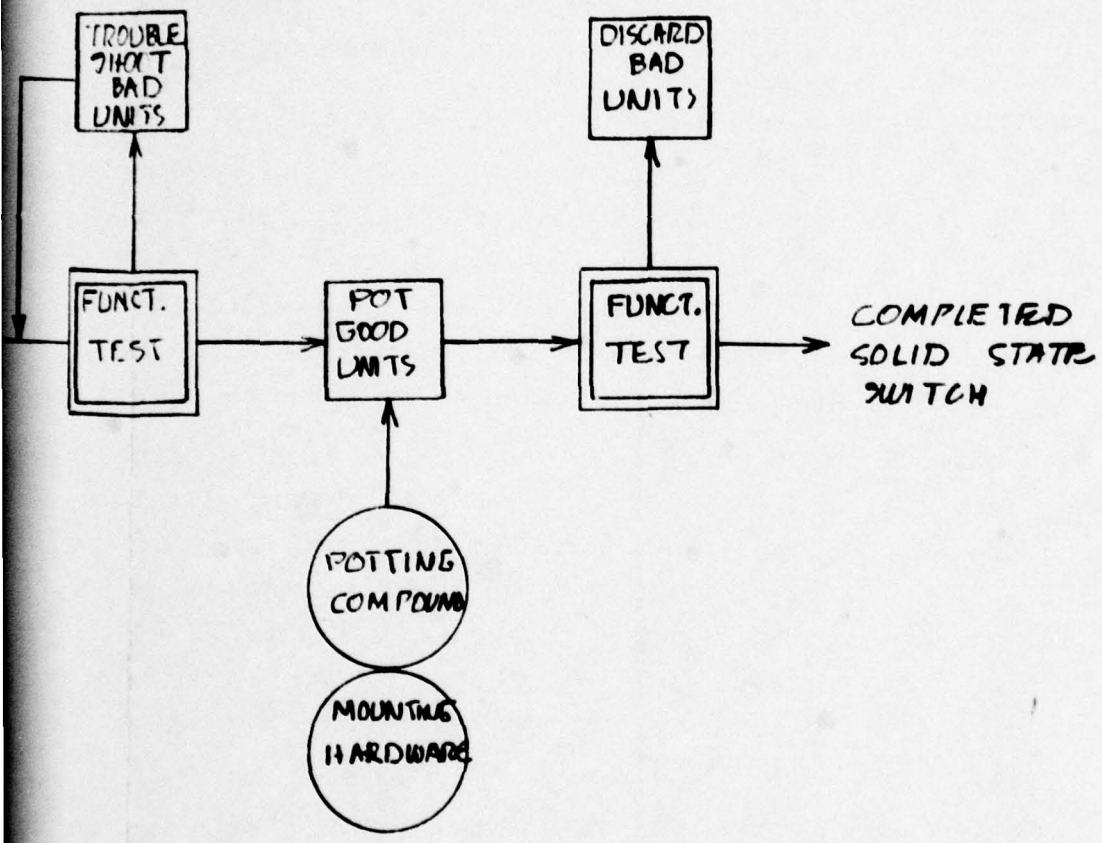

BOARD TEST
HAND SOLDERING
(2)
(14)
INSPECT & TEST OUTPUT BDS.
LOCATE & INSERT WIRES ON ONE SIDE OF CONVEYOR - CUT, CLINCH & SOLDER OTHER SIDE OF CONVEYOR
INSPECT & TEST LOGIC BDS
CONNECT CONN. WIRES TO BD
CONNECT SW. WIRES & HARNESS TO BD.
CONNECT HARNESS WIRES TO OUTPUT BD.
CONNECTOR WIRED
SWITCH WIRED
HARNESS ASSEMBLED
WIRE CUT & STRIP
PRODUCTION PROCESS
AUTOMATIC MACHIN



MATIC MACHINE AIDED PRODUCTION PROCESS

Figure 6-6. Solid State Switch Assembly Line Fl





ODUCTION PROCESS

Figure 6-6. Solid State Switch Assembly Line Flow Graph

- Component insertion
- Machine soldering, lead trimming and cleaning
- Board handling and hardware insertion
- Board test
- Hand soldering
- Assembly
- Pre pot test and trouble shooting
- Potting
- Final functional test

Each process will be discussed in the order it is accomplished on the production line.

6.2.1 COMPONENT INSERTION

An axiom of the trade is that the greater the number of insertions per pass through an automatic insertion machine, the greater will be the economical advantage in using the machine. Because of this, it will be most economical to group several small PC boards together for the insertion cycle. The point then arises as to how the boards should be grouped (i.e., output boards together, and logic boards together or output and logic boards together).

In deciding how to group the PC boards, the following points were considered:

- The output board has (19) identical axial lead components to insert which are all oriented the same. Therefore, no sequencing of these parts would be necessary and one pass through the machine would be all that is required.
- The logic board has only (8) axial lead machine insertable components in one orientation as opposed to (17) in a second orientation. The percentage of parts inserted with each pass will be closer if the logic and output boards are combined.

- One axial lead insertion machine will easily meet the required production rate. Therefore, there is no advantage in dividing the work load between two machines.

Based on these considerations, one logic board and one output board were grouped together and treated as a single board in the initial steps in this proposed production line.

Component insertion can further be categorized by component configuration as axial leads, dual-in-line pin (DIP), and non-machine insertable (manual).

a. Axial Lead

Machine insertion of axial lead components is accomplished with an insertion head that holds the individual component by its leads. The component leads are cut to remove the component from the tape reel. The insertion head forms the leads and pushes the formed leads into the board holes. Another head works from under the board to cut and clinch the leads.

One consideration in carrying out the above operation is that the head generally has a fixed orientation to the board so that only the components that are orientated the same way can be inserted in any one pass of the board through the machine.

A second consideration is that of lead span, also called center distance of each component. If the lead span is the same for all axial lead insertions a Fixed Center Distance (FCD) head can be used to insert the components. If only two lead spans exist, then a Dual Center Distance (DCD) head can be used. Another option is the Adjustable Center Distance (ACD) head. A fourth option is to use a Variable Center Distance (VCD) head to insert axial lead components; however,

a VCD machine requires computer control to position the two halves of the insertion head at the proper distance apart for each component as required.

Axial lead components will be inserted into the logic and output board combination in two passes of the X-Y table (and board) under the head as shown in Table 6.1

A total of 44 axial lead components will be inserted per logic-output board combination. To manufacture 1000 solid state switches per week (using a 35 hour week), 44,000 components will be inserted per week which is equivalent to 1260 insertions per hour.

To meet this insertion rate, a Universal 6222 Adjustable Center Distance Pantograph Insertion Machine is selected. The manufacturer claims an insertion rate of 2000 component insertions per hour.

b. DIP

As in axial lead insertion, DIPs are held in an insertion head by gripping the leads. An X-Y table moves under manual control, carrying the PC board to a series of positions as directed by a pantograph template. A more sophisticated system has the X-Y table moving under computer control to increase insertion rates.

The proper DIP for insertion is manually or automatically selected from a rack-type magazine.

A DIP insertion gun is available which feeds from a single slide magazine. The claimed insertion rate is 120 IC's per minute which would be very adequate. The process of manually positioning the gun to the proper point over the board for insertion would appear to require considerable skill, however.

FMC

TABLE 6-1 - MACHINE INSERTION OF AXIAL LEAD COMPONENTS

Pass 1	Pass 2
CR1	R2
R9	R1
R10	R22
R1	R20
R8	R5
R11	R6
R12	R3
R18	R4
R25	C8
R13	C7
R14	C6
R17	C9
R15	C4
R24	C5
R21	C2
R19	C3
R23	C1
	C10
	C11
	C12
	C13
	C14
	C15
	C16
	C19
	C18
	C17

DIP components will be inserted into the logic portion of the logic and output board combination in one pass of the X-Y table (and board) under the head in the order that follows: U4, U3, U5, U8, U2, U7, U10, U6, U9. A total of 9 DIP components will be machine inserted per logic-output board combination. 9000 components will be inserted per week which is equivalent to 258 insertions per hour. To meet this insertion rate, a Synergistic Econodip Model 2300 Pantograph Insertion Machine is selected. The manufacturer claims an insertion rate of 1000 component insertions per hour.

c. Manual

There are two basic approaches that can be taken for manual component insertion. One approach is to let one operator insert all the different components in the board. The other approach is to let one operator insert just a few components of a particular type.

The assembly approach taken here is that of a group operation, progressive line (essentially the second approach above). This is one of the most efficient methods of assembling components into a printed circuit board. A group of operators, working independently and performing an assigned set of work tasks, is utilized. A printed circuit board is conveyed from operator to operator via conveyor belt.

In-house FMC time and motion studies indicate that for this progressive line, an average of 212 components inserted per hour will be a base-line minimum.

To insert the 40 non-machine insertable components by hand will require 11.4 minutes.

To manufacture 1000 solid state switches per week, 40,000 components will be inserted per week at the

average rate of one component each 17 seconds. Therefore, 11,350 minutes or 190 hours per week will be required to complete the 1000 units.

For a 35 hour week, six people will be required to expend the 190 hours in one week.

In deciding which components will be inserted at each station the following was considered:

- For 40 components inserted and 6 people to do the inserting, each person will insert an average of 7 components, to divide the work load evenly.
- Inserting like components is more efficient than inserting un-like components.

Based on the above considerations the component insertion groupings are as shown in Table 6-2.

To create a smooth running manual insertion progressive line, the Electrovert Ipac In-Line Assembly Conveyor is specified. The conveyor rate of travel will coincide with the required production rate of 212 components inserted per hour. Boards will be loaded onto the conveyor at the loading end of the conveyor and as they move past the operators, the components will be selected from convenient bins and inserted in the printed circuit board.

The 18' Model Ipac -18 conveyor is specified. This will allow ample space for 6 operators to work at the conveyor.

TABLE 6-2 - HAND INSERTION OF COMPONENTS

Operator	Components Inserted
1	Q2, Q1, Q6, Q3, Q7, Q8
2	C21, C22, VR2, C20, C25, VR1, C24, C27, C26, C23
3	T1, T2, T3, T4, T5, T6
4	T9, T8, T7, T10, T11, T12
5	T13, T14, T15, T16, T19, T18
6	T17, U1, RT1, Q5, Q4, R16

FMC

6.2.2 MACHINE SOLDERING

There are approximately 442 individual solder points on one logic-output board combination. If one connection point is soldered each 10 seconds it will take about 74 minutes to solder one combination board. Since this is more than six times the time required for manual insertion, about 30 people would be required on a progressive line to meet the production rate. Obviously, hand soldering is not economical where a wave-solder station can be incorporated into the line.

The Ipac In-Line Assembly Conveyor specified previously is fitted with an inclinable unload to allow interfacing directly with the conveyor of a wave-soldering system. This allows completely assembled circuit boards to move from the assembly conveyor to the soldering system conveyor. With this system there will be no opportunity for components to become dislodged because of board handling.

The Electrovert Model 724 Inclinable Frame Conveyor-wave-solder System is specified to perform the printed circuit board soldering function. The conveyor speed is adjustable from 0 to 20 Ft/Min which will easily accomodate the speed required. Some component leads and/or solder may be too long on the soldered side of the board after the wave soldering process. To assure that leads are not left too long, a lead trimming process is specified in the production line at this point. The Electrovert In-Line Lead Trimmer can be interfaced with the output of the soldering system. Circuit boards will move smoothly through the lead trimmer and on to the printed circuit board cleaning process.

Fluxing which is performed as part of the soldering process, creates a film over the board which must be removed by proper cleaning. The Electrovert Aquapak In-Line Cleaning Process is specified for this production line.

6.2.3 BOARD HANDLING AND HARDWARE INSERTION.

Up to this point the logic board and the output board have actually been one large, perforated board. At this station an operator separates the two boards at the perforation and smooths the edges as necessary. The output board is then ready for inspection and test. The logic board must go through an additional step of having two internally threaded standoffs swaged into place with a manually operated bench press. FMC's time and motion studies indicate that one operator can easily separate the boards, smooth the edges, and insert and swage the two standoffs within the two minute period allotted.

6.2.4 BOARD TEST

After the boards are separated, the individual logic and output boards are inspected and functionally tested. Inspection and test of the logic and output boards can take up to 2 minutes to complete.

The output board can be tested by applying an input from a signal generator at each of 19 input points and observing the output wave shape on an oscilloscope. This certainly can be accomplished in 2 minutes, especially if a test fixture is set up to speedily sequence the step function to each input and, at the same time, sequencing through the corresponding output to the oscilloscope.

If one operator is to handle the testing of the logic boards, a specially designed, dedicated test station must be established as part of the production line. This test station will exercise all logic circuits and, at the same time, monitor outputs. The quantity of circuitry is sufficient to warrant the use of high speed automatic test methods. Test equipment of this nature (not dedicated) is available but its cost is prohibitive being in the order of $25,000.00 for one test console.

A dedicated system, having the specific purpose of testing this one logic board, could be designed and built for a fraction of this cost.

6.2.5 HAND SOLDERING AND ASSEMBLY

Certain feeder operations will be required to sustain the main progressive assembly line operation in the area of hand soldering. These are wire cutting and stripping, connector wiring, and switch wiring.

The 48 interconnecting wires can be broken down into 14 groups of different length wires. To produce these wires of different lengths will require that one operator man a wire cutting and stripping machine which is fed from a spool of continuous, insulated and tinned wire. The machine is automatic, but must be adjusted for different lengths of wires. This operator also replenishes the wire supply at the three using locations. The automatic wire cutting and stripping machine selected is a Gardner-Denver model 14YA machine, with reported production rate of 3000 pieces per hour.

The three operations using the wires are connector wiring, switch wiring, and harness assembly to the logic board. Connector and switch wiring require the soldering of 27 wires to terminals. Time and motion studies indicate that this soldering will require 30 seconds per terminal or a total of 13.5 minutes. Thus 7 operators will be required to maintain the required flow of switches and connectors.

Harness assembly to the logic and output boards requires the soldering of 69 wire connections to the printed circuit board pads. Time and motion studies indicate that 10 seconds will be required to complete each connection, therefore 690 seconds of 11.5 minutes will be required to complete the task. If each station retains one board no more then two minutes, exclusive

of board handling, then there must be approximately six operators doing wire insertion, cut-and-clinch, and hand soldering and each operator must make approximately 11.5 connections in the two minute period alloted.

Each of the 69 wire connections will actually require (3) separate operations on the assembly line.

- Stripped and tinned leads are inserted into the through holes in the connection pads.
- The leads are cut and clinched in one operation from the other side of the board.
- The leads are soldered in place on the cut and clinch side of the board.

To accomplish this total task a second progressive line is specified complete with conveyor. The logic board will be held rigidly in a fixture to allow access to both sides of the board. Inserting of leads will be accomplished from one side of the board while a second operator will perform the cut and clinch function on the other side of the board. Soldering will be accomplished in the remaining four stations.

Assembly of the output board to the logic board by moving the output board into place and fastening with two screws can be accomplished at the last station of the progressive line. The assembler can also unload the units for transport to the test area.

To accomodate 7 operators the Electrovert Ipac In-Line Assembly Conveyor is specified. The 18' model Ipac-18 will have ample operator space for two operators on one side and five operators on the other side.

6.2.6 TEST

The last opportunity to test, troubleshoot and repair the unit before potting comes at this point in the manufacturing process. A quick, easily accomplished functional test with a dedicated tester will tell whether each unit is good or not. Good units will go right into the potting process while bad units will be shunted off to be repaired. Assuming functional testing can be accomplshed in less then (2) minutes and troubleshooting and repair of bad units can be accomplished within the week by a technician other then the functional test operator, no loss of production will result from finding bad units at this point.

The functional test would consist of exercising the (19) steps through which the switch passes and observing that the required output function does occur and within the specified time. Since a good unit must sense a bad squib among the 19 and bypass it, a simulated bad squib (both shorted and open circuited) would have to be presented to each output position and proper operation observed.

No dedicated tester to perform this functional test now exists and therefore none can be specified. However, a modified version of the tester built under this program and described in paragraph 3.1.3 could be built for under $5,000.00 to perform this task.

6.2.7 POTTING

To protect components, dissipate heat and assure a rugged unit, potting of the solid state switch is specified. The potting compound used is a hard epoxy resin type. The set-up time of the compound is about 60 minutes. To mesh into a production line which requires a maximum (2) minute cycle time, a number of molds are used. The number of molds is equal to the set-up

time divided by 2 minutes or 30 molds. Now, every two minutes a unit is put into a mold and a potted unit is removed from a mold.

Three threaded inserts are positioned in the mold along with the solid state switch assembly. These threaded inserts become the means for mounting the solid state switch within a rocket launcher.

6.2.8 FINAL TEST

A final functional test of each solid state switch is the last step in the manufacturing process. The required test station to accomplish this step, again, does not exist and will have to be designed and built as a special, dedicated test station. Either the same unit designed for pre-potting test or an identical unit could be used for this test.

6.3 TEST EQUIPMENT CALIBRATION

Calibration procedures must provide for a uniform method of calibration, maintenance and issue of measuring and test equipment used in assembly line test work, and establish requirements for records pertaining to such equipment.

Calibration procedures for the dedicated testers to be designed for this production line would be prepared as part of the tester design and as a minimum would include weekly tests of the squib shorting and firing parameters and the time base for sequence timing measurements.

Test equipment used in the calibration of the dedicated testers such as timers, signal generators, and oscilloscopes would themselves be calibrated on a periodic basis against acceptable secondary standards which can be traced to the National Bureau of Standards.

After equipment is calibrated a label should be attached to the equipment which shows the date of calibration, the date after which the equipment should not be used without recalibration and the date of equipment issue.

A calibration standards laboratory must be responsible for calibration, maintenance and recording of data pertinent to all measuring and test equipment.

The calibration program must be coordinated with, and responsive to the quality program and must require direct feedback from inspection personnel with prompt notification of damaged, out-of-date calibration or malfunctioning test equipment utilized in acceptance testing.

A sample of calibration procedures and forms is presented in Appendix F.

6.4 PRODUCTION ENVIRONMENT

No special clean room or electrically noise-free environment will be required to manufacture the solid state switch. A manufacturing area compatible with electronic assembly which is relatively dust free and which has a relative low humidity will contribute to the manufacturing of reliable units, however.

A Grade 1B area as defined in FMC Standard MPC-7006 would appear to be the ideal work area for this manufacturing activity. This grade corresponds to a Type I, Class B environment as specified in FED-STD-209. A copy of this standard is presented in Appendix E.

6.5 PRODUCTION LINE COST ESTIMATE

The total equipment cost to set up this production line is estimated to be slightly over $100,000.00. A breakdown of

costs and percentage of the whole cost to accomplish each production process catagory is shown in Table 6-3.

Costs for individual pieces of equipment are given in Table 6-4.

Mosts costs were obtained from suppliers, however, some costs are estimates, based on FMC prior experience.

TABLE 6-3. PRODUCTION LINE COST ESTIMATE BREAKDOWN

PRODUCTION OPERATION	COST, DOLLARS	% OF WHOLE
Component insertion	29,960	30.0
Soldering, lead trim, and cleaning	40,350	40.0
Board handling, hardware insertion	450	0.5
Board test	6,030	6.0
Hand soldering and assembly	9,433	9.5
Functional test, troubleshoot and repair	8,000	8.0
Potting	6,000	6.0
Total	100,223	100.0%

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TABLE 6-4. EQUIPMENT LIST

PRODUCTION PROCESS	EQUIPMENT	PRODUCTION RATE units/hour	COST, dollars
Component Insertion			
Axial lead	Universal 6222 adjustable center distance Pantograph insertion machine	2,000	13,000
DIP	Synergistic 2300 Econodip manual-positioning insertion machine	1,000	11,000
Hand	Electrovert IPAC-18E inline assembly conveyor with inclinable unload		5,960
Soldering	Electrovert 724 inclinable frame conveyor inline wave solder system (12 inches with fingers)		10,350
Lead trimming	Electrovert 12-inch inline lead trimming system		12,000
Cleaning	Electrovert Aquapak inline cleaning system		18,000
Board handling and hardware insertion	Table sander		250
	Bench press		200
Board test	Hewlett Packard 120B single-channel oscilloscope		560
	Hewlett Packard 8003A general purpose pulse signal generator		470
	Special purpose, dedicated printed circuit board tester	*	5,000 (est.)
Hand soldering and assembly	Electrovert IPAC-18 inline assembly conveyor		4,515
	Manix Mark 33, MK 3A3, cut and layover pneumatic hand tool		210 (ea.)
	Weller controlled output soldering station (4 required)		46 (ea.)
	Hand tools as required		300
	Gardner-Denver Model 14YA wire cutting and stripping machine		4,225
Test (2 places)	Special purpose, dedicated printed circuit board tester	*	5,000 (est.)
	Test equipment and hand tools as required for trouble shooting and repair		3,000 (est.)
Potting	Special purpose machined forms, 30 each		100 (ea.)
	Grieve Model LO-200C laboratory oven, 30 each		100 (ea.)

*Not available

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SECTION 7
PRODUCTION UNIT COST ESTIMATE

The unit cost for the solid-state switch, manufactured in a quantity of 10,000 switches on the production line specified in Section 6, is estimated as follows:

a. Material Cost

All materials were categorized by types as listed in Table 7-1. Costs shown for one switch were actual costs incurred in building each of the five prototypes. Estimated costs for 10,000 were obtained through discussions with representative vendors for each category and not through competitive bidding which would take place when actual purchases were made. Thus, the actual cost might well be less than indicated. In particular, the quantity discount on CMOS integrated circuits does not appear reasonable as compared to other IC's. Since they account for 20% of the material cost, a better discount would be significant.

b. Electronic Parts Pre-Test

All semiconductor devices and a few selected resistors and capacitors will be pre-tested prior to delivery to the assembly line. These tests, performed by independent testing laboratories, are designed to eliminate infant mortality in the tested components as well as check for proper parameters. Tests include a visual inspection, thermal shock, burn-in at elevated temperature, and final electrical test on 100% of the components. Estimated cost for this service is from $.08 to $.20 per part depending on complexity of the test. It is estimated that $3.70 per switch would cover this testing on the selected components.

c. Labor

A tabulation of the operators required in the production line is presented in Table 7-2 A total of 32

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TABLE 7-1 - MATERIAL COSTS

Category	Quantity 1	Quantity 10,000
IC's (TTL)	$66.92	$10.04
IC's (CMOS	32.89	19.26
Capacitors	31.95	9.59
Resistors	8.35	2.67
Discrete Semiconductors	13.82	4.84
Other	163.31	40.83
Hardware	4.90	1.47
Potting	2.00	.60
Total	$324.14	$89.30

TABLE 7-2 - PRODUCTION PERSONNEL

Production Operation	NO. Operators	% of Whole
Component Insertion	8	25
Soldering, lead and cleaning	1	3.1
Board handling hardware insertion	1	3.1
Board test	2	6.3
Hand soldering and assembly	15	47
Functional test troubleshoot and repair	2 prepot 1 post-pot	9.4
Potting	2	6.3
Total	32	100%

operators are required to produce a switch in 2.1 minutes. Thus, 1.12 manhours are required per switch.

Based on the above items, the cost of the solid state switch produced in a large quantity would be:

Material	$89.30
Pre-Test	3.70
G & A at 15%	13.95
Labor (1.12 hours at $4. and 150% Burden)	11.20
Sub-Total	$118.15
Profit at 20%	23.63
Total	$141.78

If the recommendations presented in Section 2 are followed (i.e. use of a hybrid circuit, flexible circuit interconnect, and new transformer packaging) it is estimated that the unit cost for the solid state switch would be affected as follows:

a. Material Cost

The material cost would increase somewhat with the hybrid circuit estimated at $55. (from figures in Appendix B), flexible circuit interconnect with connector pre-attached at $17., and remaining hardware and components at $30., for a total of $102.

b. Electronic Parts Pre-Test

This cost would remain about the same. Although fewer components are involved, the test of the hybrid circuit would be more complicated and thus more expensive.

c. Labor

The assembly line would be considerably different for this switch. One machine operator and one hand insertion operator could handle all component insertion eliminating 6 operators in that portion of the line.

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The board handling and hardware insertion station would be eliminated as would the two inspection stations for the individual boards.

The only operation performed at the hand soldering station would be the attachment of the switch to the flex circuit. All operations involving wire cutting and stripping, harness assembly and wiring, connector wiring, and interboard wiring would be eliminated. Thus 13 operators would be eliminated at this station.

The one operator for assembling the two boards would be eliminated since there is now only one board.

This leaves a total of 11 operators to man the entire line or about .32 hours per switch.

Based on the above, the cost of this switch would be:

Material	$102.00
Pre-Test	3.70
G & A at 15%	15.86
Labor (.4 hours at $4. and 150% Burden)	3.20
Sub-total	124.76
Profit at 20%	24.95
Total	$149.71

Although this cost is slightly higher than that estimated for the presently designed solid state switch, the following facts should be considered:

a. The hybrid cost is based on the estimate received from Itek Corporation and included in Appendix B. A budgetary estimate received from another hybrid manufacturer quoted $27.75 per unit for 10,000 units and $25.35 per unit for 25,000 units. A visit to his plant gave

indication of a much lower overhead with most production involving high volume, commercial products, such as Timex electronic watch modules. Thus in competitive bidding a price for the hybrid circuit might be obtained that would drop the cost of the completed switch below that of the presently designed switch.

b. The use of flexible circuits would eliminate the possibility of any miswiring in the interconnection of connector, switch and circuit board. This will cut down on rework of miswired units and improve reliability of completed units.

c. The elimination of most of the hand operations in hardware insertion, wire stripping, and soldering automatically means an increase in reliability by eliminating the effects of operator's moods and deficiencies.

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APPENDIX A

TEST SET DESIGN

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Appendix A: Test Set Design

A basic description of the test set and its operation were presented in Paragraph 3.1.3. A photograph of the test set was presented in Figure 3-4 in Section 3.

Actual circuitry used in the test set is presented in the schematic diagram of Figure A-1. When the set is connected to a DC power source and the Power On switch turned on, voltage is applied to the Burst Select timing circuit comprised of the integrated circuit timer, U1, and associated capacitor C21, and resistors R13 through R28, and Burst Select switch, S21. Voltage is also applied to the 19 squib simulation circuits.

Closure of the trigger switch initiates the timing cycle and the output of U1 turns on Q20 and Q21 applying power to the solid state switch through the 5 Ohm resistor R32 and pin A of the connector. This power remains on until U1 times out (30 ms, 720 ms or 885 ms depending on the position of S21).

Squib fire outputs from the switch then arrive at the 19 pins as shown. A typical squib simulation circuit is shown for the squib 1 output.

With the squib select switch for squib number 1 set on "OK" the fire signal is applied through a set of normally-closed relay contacts, K1A, to the gate firing circuitry shown for Q1, a thyristor. This circuitry is chosen to fire the thyristor only if the fire signal is of sufficient amplitude and remains on the line for the minimum time specified to fire any squib which is within its prescribed tolerance.

When Q1 fires, relay K1 is energized opening contacts K1A to present a "squib fired" condition to the solid state switch and

AD-A075 761 FMC CORP SAN JOSE CA ORDNANCE ENGINEERING DIV F/G 9/5
MANUFACTURING METHODS REPORT. STATIC SWITCH.(U)
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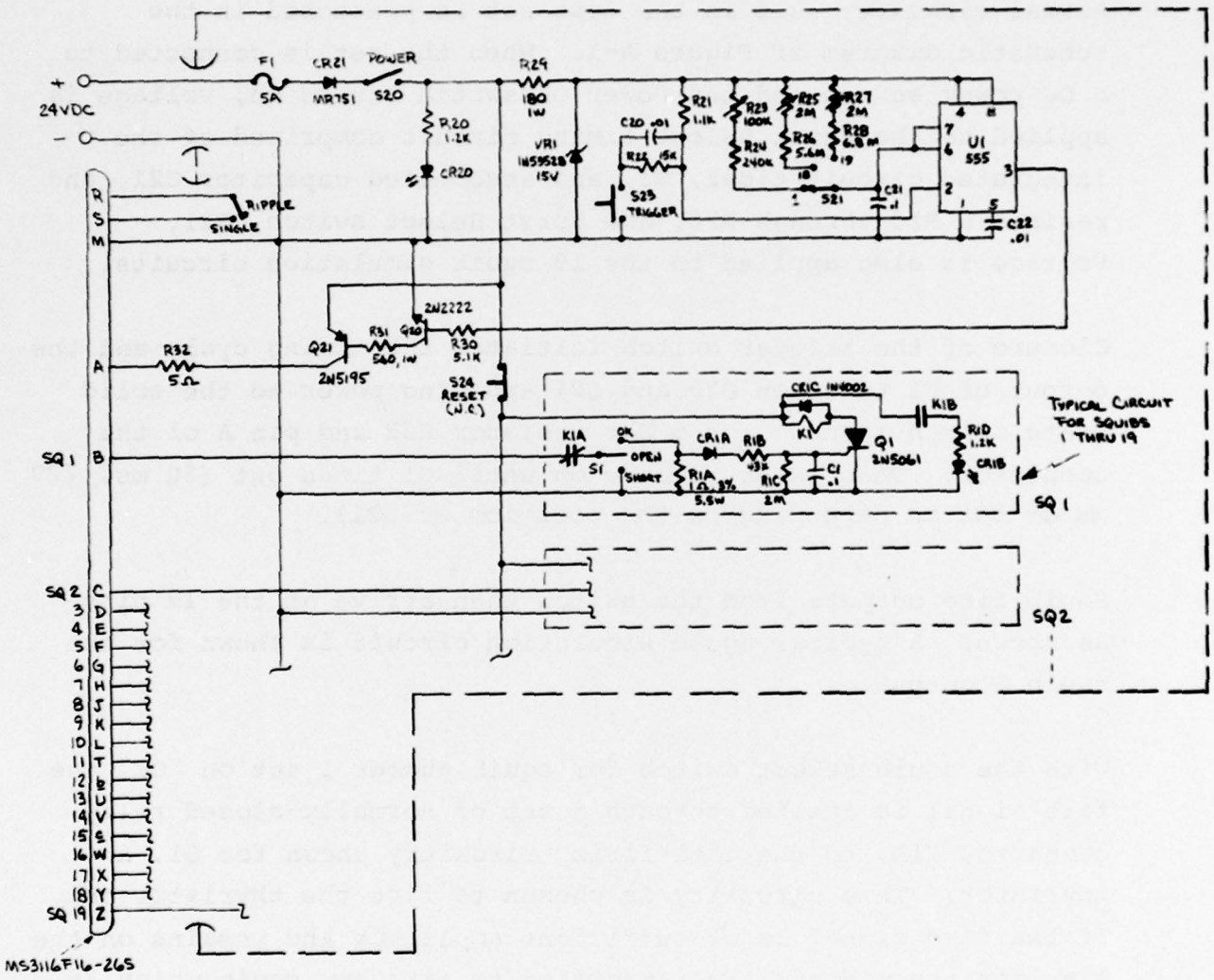

Figure A-1. Test Set Schematic Diagram

closing contacts K1B to light the indicator lamp, CR1B, showing the operator that squib number 1 has been "fired".

Pressing the Reset switch, S24, interrupts power to Q1 allowing it to regain its off state and K1 to de-energize. Thus the circuit is ready to be "fired" again.

Switch S1 can also be set in either the "Open" or "Short" position to simulate either a previously fired squib or one which has malfunctioned and is in either the open-circuited or short-circuited condition. In this way the solid state switch's capability of stepping over opens or shorts can be verified.

The Single/Ripple switch provides the same logic input to the solid state switch as the Single/Ripple switch on the actual rocket launcher.

Figures A-2 and A-3 show the interior construction of the test set with a panel for relay mounting and a circuit card for mounting of all the electronic components. The entire unit is housed in a rugged steel box with hinged, gasketed cover for environmental protection when used in the field. The two cables roll up and store within the closed box.

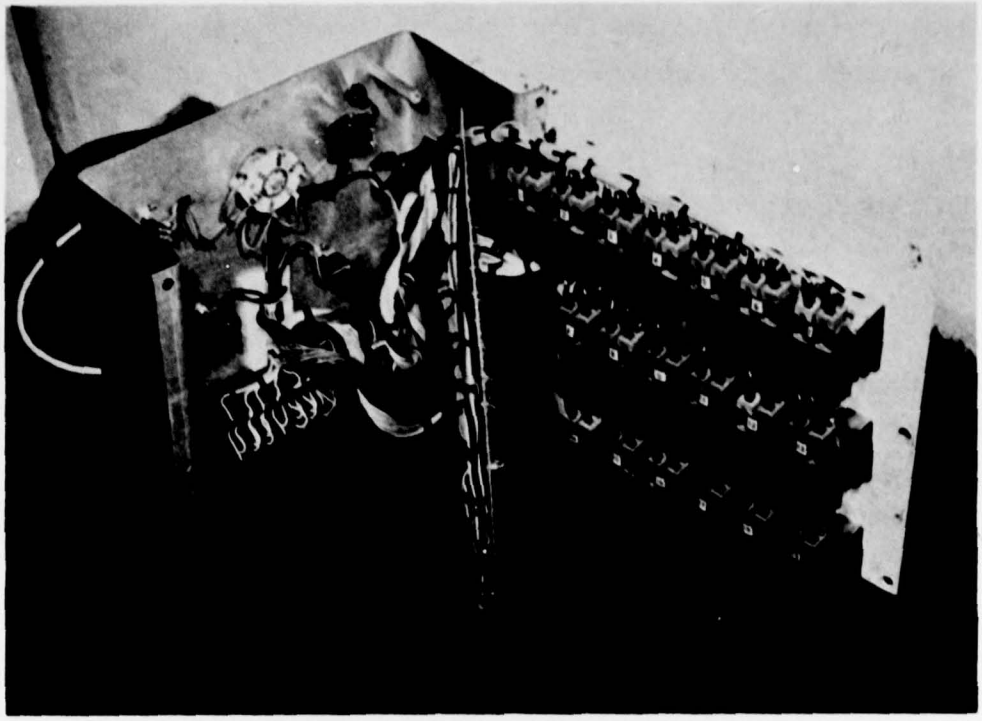

Figure A-2. Interior Construction, Relay Panel

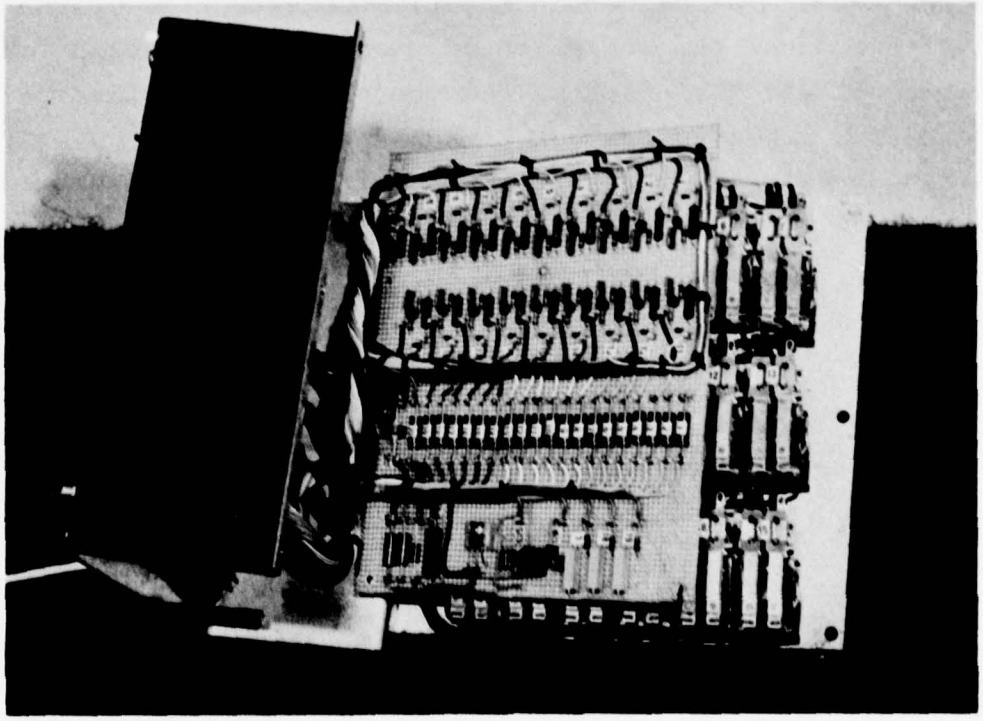

Figure A-3. Test Set - Interior Construction, Circuit Card

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APPENDIX B

HYBRID CIRCUIT INVESTIGATION

Submitted separate from this report are two sets of drawings (one reproducible) including:

Parts List, PL32-039453-01, 3 sheets
Assembly Dwg., 32-039453, 2 sheets
10:1 Artwork, 9 sheets

Copy No. _____

Itek

PRODUCTION COST PROPOSAL

For

FMC STATIC HYBRID SWITCH

In

FULFILLMENT OF FMC PO 015-B14

Applied Technology
A Division of Itek Corporation
645 Almanor Avenue, Sunnyvale, California 94086 (408) 732-2710

PRODUCTION COST ESTIMATES FOR QUANTITY 10,000 STATIC SWITCH

THE ATTACHED FLOW CHART SHOWS THE SEQUENCE IN WHICH THE FMC STATIC SWITCH HYBRIDS SHALL BE FABRICATED, ASSEMBLED AND TESTED.

BASIC ASSUMPTIONS MADE IN ESTIMATING THE DIRECT LABOR COSTS ARE:

A. ACTIVE AND PASSIVE COMPONENTS SHALL BE ATTACHED USING SPECIFIED CONDUCTIVE EPOXY.

B. SUBSTRATES SHALL BE EPOXY MOUNTED IN METAL FLATPACK PACKAGES

C. ALL BONDS FROM SEMICONDUCTOR CHIPS TO THE SUBSTRATE SHALL BE MADE USING ALUMINUM WIRE, AND BONDS FROM PACKAGE TO SUBSTRATE SHALL BE MADE WITH GOLD WIRE.

D. ELECTRICAL TESTING SHALL BE PERFORMED USING AN AUTOMATIC TEST SYSTEM, WHICH WILL HAVE SOME DIAGNOSTIC TESTING CAPABILITY.

THE DIRECT LABOR ESTIMATES GIVEN BELOW ARE OBTAINED BY DETERMINING THE YIELDED RATES FOR EACH OPERATION SHOWN IN THE FLOW CHART AND ADJUSTING BY A 95% LEARNING CURVE FOR QUANTITY OF 10,000. THE OPERATIONAL YIELDS HAVE BEEN ESTIMATED BASED ON PREVIOUS EXPERIENCE IN BUILDING SIMILAR CHIP AND WIRE TYPE HYBRID CIRCUITS.

DIRECT LABOR ESTIMATES (QUANTITY 10,000)

YIELDED ASSEMBLY TIME	1.05 HOURS EACH
YIELDED TEST, TROUBLESHOOTING TIME	.10 HOURS EACH
QUALITY ASSURANCE INSPECTION	.10 HOURS EACH
ENGINEERING SUSTAINING	.05 HOURS EACH
TOTAL	1.30 HOURS EACH

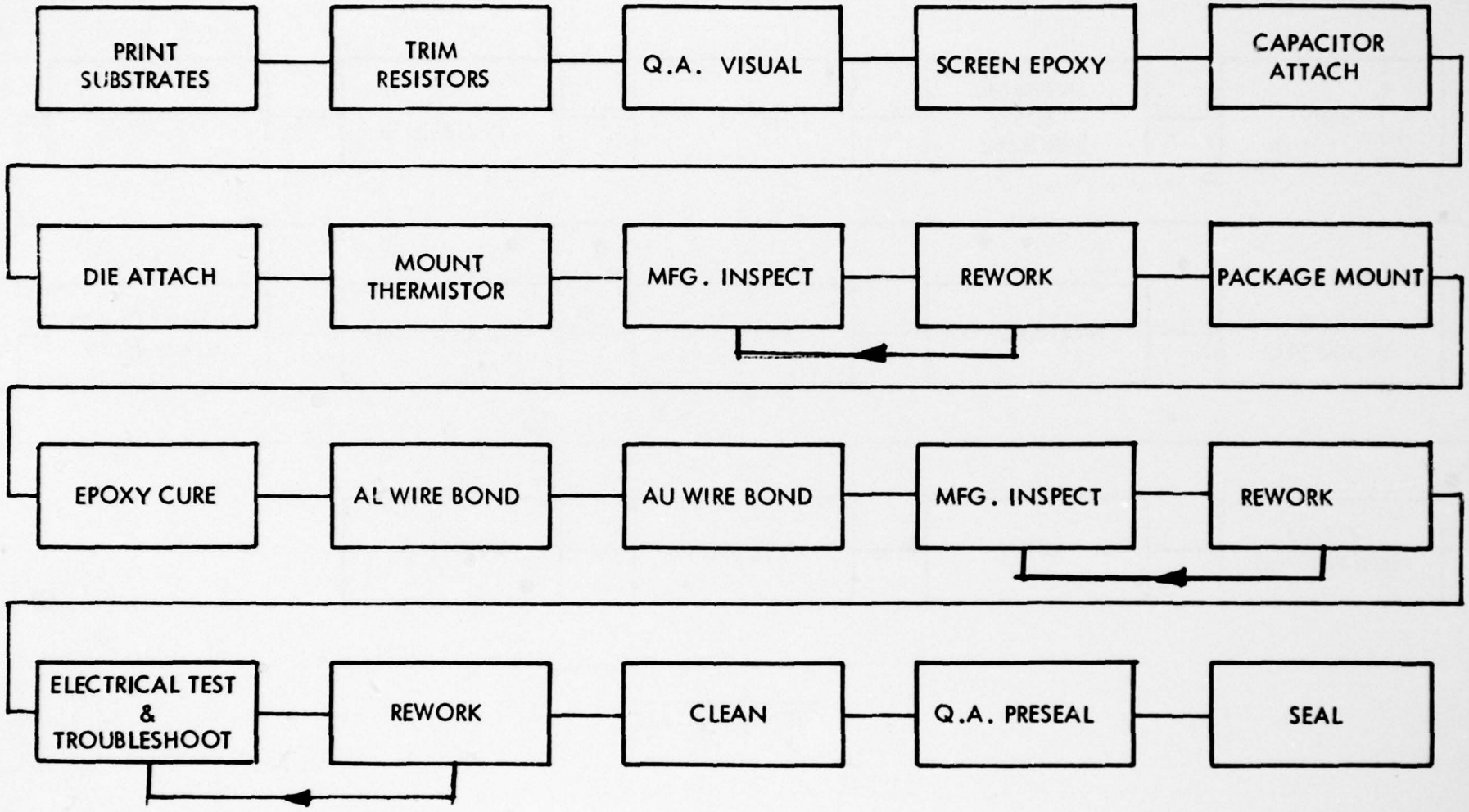
THE MATERIALS PRICES HAVE BEEN OBTAINED BY VERBAL AND WRITTEN QUOTES FROM SUPPLIERS AND FROM PREVIOUS PURCHASE ORDER HISTORY. SUFFICIENT MATERIALS HAVE BEEN PRICED TO ACCOUNT FOR OPERATIONAL YIELD LOSSES AND ALSO FOR ATTRITION AND REWORK OF THE HYBRIDS.

DIRECT YIELDED MATERIALS COST @ QUANTITY 10,000 = $49.27 EACH

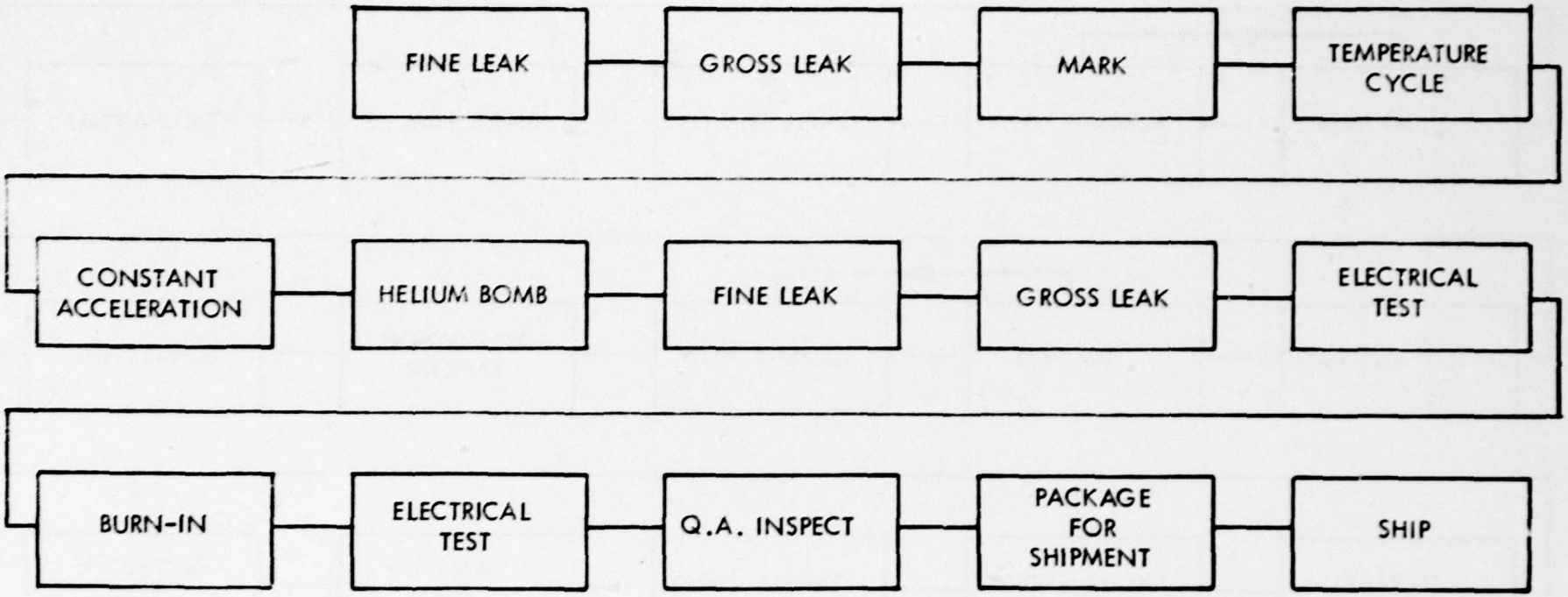
(DETAILED MATERIALS COST BREAKDOWN IS ATTACHED.)

STATIC SWITCH

HYBRID BUILD FLOW CHART



STATIC SWITCH



MATERIALS ESTIMATE SHEET

FMC STATIC SWITCH

PART NUMBER		Qty/Ckt	Quantity	Each	TotalS
Cum Yield Assembly	79%				
Cum Yield, Print & Trim	67%				
Attrition for Active Parts	15%				
Attrition for Passive Parts	10%				
Cap., 1.5 μF Tant.	20V	1	13,924	.50	6,962
Cap., .01 μF K1200	200V	2	27,848	.11	3,063
Cap., 100 PF NPO	500V	1	13,924	.13	1,810
Cap., 100 PF NPO	200V	1	13,924	.13	1,810
Cap., 15 ρF NPO	20V	1	13,924	.13	1,810
Diode 1N4001	Motorola	1	14,557	.12	1,747
2N2907	T.I.	4	58,227	.10	5,823
2N2222	T.I.	2	29,113	.09	2,620
2N4918	Motorola	1	14,557	.76	11,063
SE555V	Signetics	1	14,557	.66	9,608
DM5474	National	1	14,557	.40	5,823
CD4040A	SSI	1	14,557	1.86	27,076
CD4068B	SSI	1	14,557	.17	2,475
CD4078B	SSI	1	14,557	.17	2,475
DM54163	National	1	14,557	.93	13,538
CD4011A	SSI	1	14,557	.28	4,076
CD4009A	RCA	1	14,557	1.75	25,475
DM5445	National	2	29,113	5.00	145,565
Package	Isotronics	1	13,924	12.50	174,050
Cover	S.S.E.C.	1	13,924	1.00	13,924
Substrate	American Lava	1	15,000	.20	2,785
4 Resistor Chips	M.S.I.	4	13,924	.25	3,481
Thermistor Chip	Fenwal	1	14,557	.11	1,645
TOTAL COST					$ 482,242

CONCLUSION

THE DIRECT LABOR HOURS AND THE DIRECT MATERIALS COST GIVEN ABOVE CAN BE CONSIDERED AS THE COSTS THAT ANY TYPICAL CUSTOM HYBRID MANUFACTURER SHALL HAVE TO INCUR IN BUILDING THE 10,000 STATIC SWITCH HYBRID CIRCUITS. TO FURTHER REDUCE THE DIRECT COST ELEMENTS, TWO ADDITIONAL FACTORS CAN BE ASSUMED APPROPRIATE TO A VOLUME PROCUREMENT.

1) SELECTION OF A LOWER COST PACKAGE (PLASTIC/ CERAMIC) WOULD REDUCE THE DIRECT MATERIAL COST BY APPROXIMATELY 20%.

2) USE OF AUTOMATIC VS MANUAL WIRE BONDERS WOULD REDUCE THE ASSEMBLY LABOR TIME BY 25%.

WHILE THE ACTUAL SELLING OR PURCHASE PRICE OF THE STATIC SWITCH HYBRIDS WILL BE DETERMINED BY SUCH FACTORS AS THE SPECIFIC LABOR RATES AND OVERHEAD LOADINGS OF THE HYBRID MANUFACTURE SELECTED, IT IS ESTIMATED (CONSISTENT WITH THE ABOVE CONSIDERATIONS) THAT THE UNIT PRICE FOR PURCHASE QUANTITIES OF 10,000 CIRCUITS, WOULD BE $55.00 TO $60.00 EACH.

Copy No. _____

Itek

RELIABILITY PREDICTION

For

FMC STATIC HYBRID SWITCH

In

FULFILLMENT OF FMC PO 015-B14

Applied Technology
A Division of Itek Corporation
645 Almanor Avenue, Sunnyvale, California 94086 (408) 732-2710

TABLE OF CONTENTS

1.0 INTRODUCTION

This report presents the estimated Reliability Prediction predicated on a prototype microcircuit hybrid design, ATD P/N 32-039453. The prediction utilizes the latest math model computation to assess the reliability of the microcircuit under specified environmental conditions. The estimate is based upon only a single point estimate for microcircuits (failure/10^6 hours) and contains no acceleration factors for temperature or other environmental considerations. The failure rate values used for the semiconductor components were as of 1974.

2.0 MATH MODEL

A math model was derived utilizing the microcircuit design and selected components and their predictable performance from known parameters. The derivation of the microcircuit failure rate was based on the following equations and math model factors.

$$\lambda_P = \lambda_S + A_S\lambda_C + \Sigma\lambda_{RT}N_{RT} + \Sigma\lambda_{DC}N_{DC} + \Sigma\lambda_{PF}\pi_{PF}(\pi_T \times \pi_Q \times \pi_E \times \pi_F)$$

where:

π_Q = Quality Factor (1 used in the prediction), accounts for affects of different quality levels.

π_T = Temperature Factor accounts for package mounting base temperature, $T = e^X$.

π_E = Environmental Factor is the application environment multiplier and accounts for the influence of environmental factors other than temperature.

π_F = Circuit Function Factor - adjusts the model to account for the influence of the family type, 0.8 for digital, 1.0 for linear, 1.1 for linear-digital combination hybrids.

λ_S = Failure ratio due to substrate and film type processing (thick or thin).

$A_S \lambda_C$ = Is failure rate contribution due to network complexity and substrate area, A_S.

$\Sigma N_{RT} \lambda_{RT}$ = Is the sum of the failure rate, λ_{RT}, for each resistor as a function of the required resistance tolerance.

$\Sigma \lambda_{DC} N_{DC}$ = Is the sum of the attached device failure rates, λ_{DC}, for semiconductors, integrated circuits, capacitors, resistors, etc. both packaged and unpackaged.

$\lambda_{PF} \pi_{PF}$ = Is the hybrid package failure rate, a function of the package style or configuration and materials used in its construction.

λ_{PF} = Is a normalized value of base failure rate for all hybrid packages.

π_{PF} = Is the adjustment factor which modifies λ_{PF} as a function of package style.

EQUATIONS

$$\lambda_P = \lambda_b (\pi_T \times \pi_E \times \pi_Q \times \pi_F), \text{ failures / } 10^6 \text{ hours}$$

$$\lambda_b = \lambda_S + A_S \lambda_C + \Sigma \lambda_{RT} N_{RT}, \text{ Substrate Contribution}$$

$$+ \lambda_{DC} N_{DC}, \text{ Attached Components}$$

$$+ \lambda_{PF} \pi_{PF}, \text{ Package}$$

$$\lambda_P = \pi_L \pi_Q (C_{1AB} \pi_{T2} + C_2 \pi_E) \text{ CMOS \& IC Contribution}$$

$$\pi_T = e^X$$

$$\lambda_C = 2.4\,(10)^{-14} \left(\frac{NE}{A_S}\right)^{4.429}$$

3.0 CIRCUIT PARAMETERS

Hybrid Microcircuit -	thick-film
Ceramic Al_2O_3 Substrate -	1 inch x 2 inches
Substrate Thickness -	0.025 inch
Kovar Metal Flat Pack -	leads
Temperature Factor -	60°C
Specification Control Level -	Class B
No. of Lead Terminations -	336
No. of Thick-Film Resistors -	21
No. of Chip Devices -	24
Chip Resistors - 4	
Chip Capacitors - 6	
Diodes - 1	
Transistors - 4	
CMOS Integrated Circuits - 9	

4.0 PREDICTION CALCULATION

A_S	- 2 in^2	N_E / A_S	- 191
π_Q	- 1	λ_C	- 0.010
π_T	- 2.4	$A_S \lambda_C$	- 0.020
π_E	- 4.0	λ_T	- 5×10^{-4}
π_F	- 1.1	$\Sigma N_{RT} \lambda_{RT}$	- 1.05×10^{-2}
N_{RT}	- 21	$\Sigma \lambda_{PF} \pi_{PF}$	- 1.0×10^{-2}
N_{DC}	- 25	$\Sigma N_{DC} \lambda_{DC}$	- 5.98×10^{-1}
N_{LT}	- 336	π_F	- 1.1
N_E	- 382 ($N_E = N_{RT} + N_{LT} + N_{DC}$)		

Device Description	Failure Rate λ_{DC} / 10^6 hours
Capacitors K1200 & NPO	4×10^{-4}
Diode Switching	4.8×10^{-3}
Transistor, PNP	5.3×10^{-3}
Transistor, NPN	7.7×10^{-3}
CMOS & IC's	5.8×10^{-1}

$$\lambda_b = \lambda_S + A_S \lambda_C + \Sigma N_R \lambda_{RT} = 5 \times 10^{-2}$$

$$+ \Sigma \lambda_{DC} N_{DC} = 5.98 \times 10^{-1}$$

$$+ \lambda_{PF} \pi_{PF} = 1 \times 10^{-2}$$

$$\lambda_P = \lambda_b (\pi_E \times \pi_Q \times \pi_T \times \pi_F)$$

$$\lambda_P = 5.98 \times 10^{-1} + 5 \times 10^{-2} + 1 \times 10^{-2} (4 \times 1 \times 2.4 \times 1.1)$$

$$\lambda_P = 6.7 \text{ f} / 10^6 \text{ Hours}$$

5.0 TIME TO FAILURE (TTF)

$$\lambda_P = 6.7\ f / 10^6 \text{ hours}$$

or: 1 failure / 142,000 hours

or: 1 failure / 16 years

6.0 CONCLUSIONS

The results of the Reliability Prediction indicates a life expectancy of 142,000 hours before circuit failure. Techniques for improving the life expectancy estimate includes reduction in operation temperature, use of Hi-Rel Class A semiconductor, and circuit redundancy. A detailed trade-off would be required to determine what combination of techniques and components would produce the most upgrading.

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APPENDIX C

CIRCUIT STRESS ANALYSIS SHEETS

CIRCUIT STRESS ANALYSIS

ASSEMBLY NAME:	NUMBER:	SUBASSEMBLY NAME:	NUMBER:	ANALYST:	DATE:	PAGE OF
STATIC SWITCH				RAF	12/10/75	1 | 4

CIRCUIT SYMBOL	PART DESCRIPTION:	RATING	APPLIED STRESS			COMMENTS:	STRESS RATIO	FAIL RAT PER 10 HI
			D.C.	A.C.	TRANS.			
C1-C19	Capacitor, Tant., 4.7μf	10V	2V			19@ 0.03×10^{-6}	0.2	0.572
C20	Capacitor, Tant, 4.7μf	10V	5V				0.5	0.255
C21	Capacitor, Tant, 4.7μf	50V	30V				0.60	0.375
C22	Capacitor, Tant., 1.5μf	20V	18V				0.90	1.110
C23	Capacitor, Ceramic, .01μf	200V	5V				<0.1	0.024
C24	Capacitor, Mica, 100pf	500V	5V				<0.1	0.011
C25	Capacitor Ceramic, .01μf	200V	5V				<0.1	0.024
C26	Capacitor, Ceramic, 100pf	200V	5V				<0.1	0.024
C27	Capacitor, Tant., 15μf	20V	5V				0.25	0.008
C28	Capacitor, Tant., 0.22μf	100V	18V				0.18	0.099
CR1	Diode, Rectifier	1A	1.64mA				<0.1	2.415
J1	Connector, 26 pin					24 active pins		0.176
R1	Resistor, Carb. Comp. 10K	0.25W	2.07mW				<0.1	0.001

C-1

CIRCUIT STRESS ANALYSIS

ASSEMBLY NAME:	NUMBER:	SUBASSEMBLY NAME:	NUMBER:	ANALYST:	DATE:	PAGE OF
STATIC SWITCH				RAF	12/28/75	214

CIRCUIT SYMBOL	PART DESCRIPTION:	RATING	APPLIED STRESS			COMMENTS:	STRESS RATIO	FAIL RATE PER 10^6 HR
			D.C.	A.C.	TRANS.			
R2	Resistor, Carb. Comp, 1K	0.25W	2.07mW				<0.1	0.001
R3	Resistor, Film, 2K	0.125W	12.5mW				0.1	0.003
R4	Resistor, Film, 51K	0.125W	0.4mW				<0.1	0.003
R5	Resistor, Carb Comp, 10K	0.25W	2.5mW				<0.1	0.001
R6	Resistor, Carb Comp, 430	0.25W	58.2mW				0.23	0.001
R7	Resistor, Carb. Comp, 1K	0.25W	21mW				<0.1	0.001
R8	Resistor, Carb Comp, 430	0.25W	9.3mW				<0.1	0.001
R9	Resistor, Carb. Comp, 91	0.25W	194mW				0.78	0.003
R10	Resistor, Carb. Comp, 430	0.25W	9.3mW				<0.1	0.001
R11	Resistor, Carb. Comp, 1K	0.25W	21mW				<0.1	0.001
R12	Resistor, Carb. Comp, 91	0.25W	194mW				0.78	0.003
R13	Resistor, Carb Comp, 100	0.25W	67mW				0.27	0.001
R14	Resistor, Carb. Comp, 10K	0.25W	27mW				0.11	0.001
R15	Resistor, Carb Comp, 3K	0.75W	8.1mW				<0.1	0.001
R16	Resistor, Carb Comp, 100	0.75W	67mW				0.27	0.001
R17	Resistor, Carb Comp, 10K	0.25W	23mW				<0.1	0.001

CIRCUIT STRESS ANALYSIS

ASSEMBLY NAME:	NUMBER:	SUBASSEMBLY NAME:	NUMBER:	ANALYST:	DATE:	PAGE OF
STATIC SWITCH				RAF	12/20/[illegible]	3 14

CIRCUIT SYMBOL	PART DESCRIPTION:	RATING	APPLIED STRESS D.C.	APPLIED STRESS A.C.	APPLIED STRESS TRANS.	COMMENTS:	STRESS RATIO	FAIL RATE PER 10 HR
R18	Resistor, Carb Comp, 1K	0.25W	2.3mW				<0.1	0.001
R19	Resistor, Carb Comp, 2.2	0.25W	4mW				<0.1	0.001
R20	Resistor, Carb Comp, 2.2	0.25W	12.3mW				<0.1	0.001
R21	Resistor, Carb Comp, 16	0.25W	59.5mW				0.24	0.001
R22	Resistor, Carb Comp, 270	0.25W	131mW				0.52	0.001
R23	Resistor, Carb Comp, 510	0.25W	247mW				0.99	0.005
R24	Resistor, Carb Comp, 1K	0.25W	19.4mW				<0.1	0.001
Q1	Transistor, PNP, 2N2907	400mW V_{CE}=40V	30mW 18V				<0.1 0.45	0.818
Q2	Transistor, PNP, 2N2907	400mW V_{CE}=40V	27.2mW 18V				<0.1 0.45	0.818
Q3	Transistor, PNP, 2N2907	400mW V_{CE}=40V	231mW 5V				0.58 0.125	0.615
Q4	Transistor, PNP, 2N2907	400mW V_{CE}=40V	231mW 5V				0.58 0.125	0.615
Q5	Transistor, NPN, 2N2222	500mW V_{CE}=50V	30mW 18V				<0.1 0.45	0.900
Q6	Transistor, PNP, 2N4918	30W V_{CE}=40V	1.35W 18V				<0.1 0.45	4.092
Q7	Transistor, NPN, 2N4921	30W V_{CE}=40V	1.35W 18V				<0.1 0.45	4.092
Q8	Transistor NPN 2N2222	500mW V_{CE}=50V	49mW 5V				<0.1 0.1	0.126

CIRCUIT STRESS ANALYSIS

ASSEMBLY NAME:	NUMBER:	SUBASSEMBLY NAME:	NUMBER:	ANALYST:	DATE:	PAGE OF
STATIC SWITCH				RAF	12/28/75	4 | 4

CIRCUIT SYMBOL	PART DESCRIPTION:	RATING	APPLIED STRESS			COMMENTS:	STRESS RATIO	FAIL RATE PER 10^6 HR
			D.C.	A.C.	TRANS.			
S1	Switch, Rotary							6.030
T1-T19	Transformer					19 @ 0.048		0.912
U1	IC, SE555V, MonoMV							9.200
U2	IC, SN5474, Binary FF							11.538
U3	IC, CD4040, Binary Ctr.							27.900
U4	IC, CD4068, 8-Inp. NAND							6.404
U5	IC, CD4078, 8-Inp. NOR							6.404
U6	IC, SN54103, Binary Ctr.							21.975
U7	IC, CD4001, 2-Inp. NOR							6.404
U8	IC, CD4009, Hex. Inv.							7.499
U9	IC, SN5445, BCD/DIC DEC							14.040
U10	IC, SN5445, BCD/DIC DEC.							14.040
VR1	IC, Volt. Reg, 5V							21.620
VR2	IC, Volt. Reg, 18V							21.620

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APPENDIX D

EMI REFERENCES

AND TEST DATA

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APPENDIX D - REFERENCES AND EMI TEST DATA

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The test data presented in the following pages is the raw data recorded in tests up to the time of submittal of this report. A complete report of the tests will be forwarded upon receipt from the subcontracted test facility.

PHILCO

PHILCO FORD CORPORATION

TEST DATA SHEET

TEST NO. 76EMC69

DATE MARCH 18, 1976

SHEET 1 OF 1

CURVE

TEST SAMPLE: AIRCRAFT ROCKET LAUNCHER

MODEL NO: LAU 61A/A SERIAL NO: 2

TEST: RADIATED SUSCEPTIBILITY WITH 1.5' INTERV

RI-FI METER: DETECTOR FUNCTION:

SPECIFICATION:

NOTES:
1) LONGEST LEADS, SIG, TUBE-CA
2) < RCVR NOISE LEVEL

FREQ (MHz)	FIELD LEVEL (V/M)	CIRCUIT VOLTAGE (dBuV)	CT-1 FACTOR (dB)	PROBE CURRENT (dBuA)				SPEC LIMIT (dBuA)
0.030	200	<14	-14	<0				90
0.100	200	<14		<0				
0.250	200	<14		<0				
0.535	200	<6		<-8				
2.0	200	10		-4				
32	200	41		27				
100	200	29		15				
196	200	34	-14	20				90

Q.A. ENGINEER Clayton E. Doggett

DATE: Robert Cannon

PHILCO
PHILCO-FORD CORPORATION

TEST DATA SHEET

TEST NO. 76EMC69
DATE MARCH 19, 1976
SHEET 1 OF 5
CURVE

TEST SAMPLE: AIRCRAFT ROCKET LAUNCHER
MODEL NO: LAU 61 A/A SERIAL NO: 2
TEST: RADIATED SUSCEPTABILITY WITH 5% INTERV
RI-FI METER: N/A DETECTOR FUNCTION: NA
SPECIFICATION:

NOTES:
1) LONG LEADS
2) PHYSICAL CONF. - HANGARS UP
3)

FREQUENCY (MHz)	FIELD LEVEL (v/M)	CIRCUIT VOLTAGE (dBuV)	CT-1 FACTOR (dB)	SQUIB CURRENT (dBuA)	SQUIB CURRENT PROJECTED TO TEST PLAN FIELD INTENSITY REQUIREMENTS dBuA	mA	TEST CONDITION	
32	200	41	-14	27	27	0.022	LOAD/ARM	SW TO LOAD
32	200	41	-14	27	27	0.022	LOAD/ARM	SW TO ARM
31		37		23	23	0.014		
30		34		20	20	0.010		
29		31		17	17	0.007		
28		26		12	12	0.004		
26		32		18	18	0.008		
24		22		8	8	0.003		
22		27		13	13	0.005		
20		33		19	19	0.009		
16		32		18	18	0.008		
12		30		16	16	0.006		
10	200	29	-14	15	15	0.006	LOAD/ARM	SW TO ARM
32	200	41	-14	27	27	0.022	LOAD/ARM	SW TO ARM
33	200	41		27	27	0.022		
34	160	40		26	28	0.025		
35	140	39		25	28	0.025		
36	130	39		25	28	0.025		
38	100	41		27	33	0.045		
40	100	42		28	34	0.05		
42	175	40		26	27	0.022		
44	90	62		48	55	0.562		
43	70	55		41	49	0.282		
46	200	53		39	39	0.057		
50	160	36		22	24	0.016		
55	110	44		30	35	0.056		
60	200	45		31	31	0.035		
70	200	37		14	14	0.005		
80	200	46		32	32	0.040		
90	140	30		16	19	0.009		
100	150	29	-14	15	17	0.007	LOAD/ARM	SW TO ARM

Q.A. _____ ENGINEER Clayton E. Doggett

DATE: _____ D-4 _____

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TEST DATA SHEET

TEST NO. 76E mc 69

DATE MARCH 19, 1976

SHEET 2 OF 5

CURVE

TEST SAMPLE: AIRCRAFT ROCKET LAUNCHER

MODEL NO: LAU 61 A/A SERIAL NO: 2

TEST: RADIATED SUSCEPTABILITY WITH SS INTERF

RI-FI METER: DETECTOR FUNCTION:

SPECIFICATION:

NOTES:
(1) CONN. LEADS
(2) SWITCHED TO ARM
(3) HANGARS UP - CONFIGURATION

FREQ. (MHZ)	FIELD LEVEL (V/M)	CIRCUIT VOLTAGE (dBuV)	CT-1 FACTOR (dB)	SCUTA CURRENT (dBuA)	PROJECTED SCUTA I. TO TEST PLAN LEVELS (dBuA)	TEST CONDITION
32	200	41	-14	27	27	
32	180	40		26	27	
32	160	39		25	27	NOTES (1) (2) & (3)
32	140	38		24	27	
32	120	37		23	27	
32	100	35	-14	21	27	
32	200	71	-14	57	57	NOTES 1, 2 & 3
44	90	87		73	86	AND AIRCRAFT POWER
100	200	95		81	81	CABLE CONNECTED
43	70	88		74	83	(6' of LOOPED WIRE
42	170	85	-14	71	73	ON A CURVE)
100	200	30	-14	16	16	PWR CABLE REMOVED - CONN. CAPPED
100	200	32	-14	18	18	PWR CABLE REMOVED - NOT CAPPED
100	190	21	-14	7	8	TEST CONFIGURATION
44	160	27		13	15	CHANGED TO - INTERF
32	200	14	-14	0	0	ACCESS DOOR OPEN
						NOTES 1 & 2 SAME

Q.A. ENGINEER Clayton E. Doggett

DATE: D-5 Robert Arvin

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PHILCO FORD CORPORATION

TEST DATA SHEET

TEST NO. 76EMC69

DATE MARCH 19, 1976

SHEET 3 OF 5

CURVE

TEST SAMPLE: AIRCRAFT ROCKET LAUNCHER

MODEL NO: LAU 61 A/A SERIAL NO: 2

TEST: RADIATED SUSCEPTIBILITY WITH SS INTERV

RI-FI METER: 8556/8552 DETECTOR FUNCTION: RMS-PEAK

SPECIFICATION:

NOTES:
1) SHORT LEADS
2) SWITCHED TO ARM
3) POWER CONNECTOR CAPPED
4) HANGARS UP
5) < = NOISE LEVEL

FREQ (MHz)	FIELD LEVEL (V/M)	CIRCUIT VOLTAGE (dBμV)	ET-1 FACTOR (dB)	SQUIB CURRENT (dBμA)				
0.030	200	<12	-14	<-02				
0.100	200	<12		<-2				
0.250	300	<2		<-12				
0.535	300	<2		<-12				
2.0	200	11		-3				
32	200	45		31				
100	200	34		20				
196	200	49	-14	35				

Q.A. _____ ENGINEER Clayton E. Doggett

DATE: _____ Robert Arcaini

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TEST DATA SHEET

TEST NO. 76EMC69
DATE MARCH 19, 1976
SHEET 4 OF 5
CURVE

TEST SAMPLE: AIRCRAFT ROCKET LAUNCHER
MODEL NO: LAU 61 A/A SERIAL NO: 2
TEST: RADIATED SUSCEPTIBILITY WITH 55' INTERV
RI-FI METER: _____ DETECTOR FUNCTION: _____
SPECIFICATION: _____

NOTES:
1) SHORT LEADS
2) SWITCHED TO ARM
3) HANGARS UP
4) CONNECTOR CAPPED
5) PROJECTED TO SPEC REQUIREMENTS

FREQ. (MHz)	FIELD LEVEL (V/M)	CIRCUIT VOLTAGE (dBmV)	CT-1 FACTOR (dB)	SQUIB CURRENT (dBmA)	PROJECTED SQUIB CURRENT ⑤ (dBmA)			
32	200	46	-14	32	32			
40	100	35		21	27			
44	200	55		44	44			
50	130	25		14	18			
60	200	16		2	2			
70	200	24		15	15			
80	200	44		30	30			
90	170	31		17	19			
100	200	37		23	23			
110	80	19		5	13			
120	200	32		18	18			
130	200	33		19	19			
140	200	41		27	27			
150	200	58		44	44			
160	200	41		27	27			
170	190	54		40	41			
180	200	48		34	34			
190	200	53		39	39			
200	120	42		25	32			
210	50	30	-14	16	24			

Q.A. _____ ENGINEER Clayton E. Doggett
DATE: _____ Richard E. Bossing

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PHILCO FORD CORPORATION

TEST DATA SHEET

TEST NO. 76 EMC 69
DATE MARCH 19, 1976
SHEET 5 OF 5
CURVE

TEST SAMPLE: AIRCRAFT ROCKET LAUNCHER
MODEL NO: LAU 61 A/A SERIAL NO: 2
TEST: RADIATED SUSCEPTIBILITY WITH EM INTERF
RI-FI METER: DETECTOR FUNCTION:
SPECIFICATION:

NOTES:
1) LONG LEADS
2) ARMED RDS.
3) HANGARS UP
4) CONN. CAPPED

FREQ. (MHz)	FIELD LEVEL (V/M)	CIRCUIT VOLTAGE (dBμV)	CT-1 FACTOR (dB)	SQUIB CURRENT (dBμA)	PROJ. SQUIB CURRENT TO SUSC LEVELS (dBμA)			
0.03	200	24	-14	10	10			
0.100	200	25		11	11			
0.250	200	21		7	11			
0.535	200	12		-2	2			
2	200	23		9	9			
32	200	29		15	15			
100	200	30		16	16			
196	200	53		39	39			
44	200	59	-14	45	45			

Q. A.
DATE:

ENGINEER Waylon E. Doggett
Robert Benson

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TEST DATA SHEET

TEST NO. 76 EMC 69
DATE MARCH 30, 1976
SHEET 1 OF 1
CURVE

TEST SAMPLE: AIRCRAFT ROCKET LAUNCHER
MODEL NO: LAU 61 A/A SERIAL NO: 2
TEST: RADIATED SUSCEPTIBILITY WITH 'SS' INTERV
RI-FI METER: DETECTOR FUNCTION:
SPECIFICATION:

NOTES:
ANT POS. A - 1 METER FROM REAR
B - " " AFT/PORT
C - " " FWD/PORT
LONG LEAD CONFIGURATION
(1) INCLUDES: 30' RG55 COAX, 3 dB PAD, PRE-AMP, VOLTAGE PROBE AND CONNECTORS

FREQ. (GHz)	FIELD LEVEL (V/M)	ANTENNA POSITION	DETECTED VOLTAGE LEVEL (dBµV)	MEASURING SYSTEM CORR. FACTOR (dB)(1)	CORRECTED VOLTAGE LEVEL (dBµV)	EQUIPMENT SQUIB CURRENT AT 1 OHM dBµA	SQUIBB CURRENT WORST CASE (mA)	SQUIB CURRENT PROJECTED TO SPEC AND SCALE (dBµA)	(mA)
1.0	120	A	72	-8	80	80	10	84	15.5
1.0	120	B	58	-8	66	66	2	70	3.2
1.0	120	C	59	-8	67	67	2		
1.535	50	A	47	-9	56	56	0.62	68	2.4
1.535	50	B	41	-9	50	50	0.32		
1.535	50	C	35	-9	44	44	0.16		
1.90	50	A	52	-11	63	63	1.4	75	5.5
1.90	50	B	52	-11	63	63	1.4		
1.90	50	C	46	-11	57	57	0.7		
2.35	100	A	95	+17	78	78	8	93	44
2.35	100	B	83	+17	66	66	2		
2.35	100	C	82	+17	65	65	1.8		
7.0	100	A	67	+6	61	61	1.1	75	5.5
7.0	100	B	63	+6	57	57	0.7		
7.0	100	C	50	+6	44	44	0.16		
5.4	100	A	75	+4	71	71	3.6	81	22
5.7	90	↓	88	+4	84	84	15.5	101	110
6.0	80		85	+12	73	73	4.3	93	44
6.5	120		85	+10	75	75	5.6	88	25
7.0	120		77	+6	71	71	3.5	85	17.5
7.5	95		75	+5	70	70	3.2	88	25
8.0	130		72	+2	70	70	3.2	85	17.5
8.5	85	↓	67	-11	78	78	8	96	63
~~[illegible]~~	~~[illegible]~~	~~A~~	~~[illegible]~~	~~-15~~	~~120~~	~~100~~	~~100~~		
9.0	85	A	57	-15	72	72	4	90	30
(2) 1.0	120	B	63	-8	71	71	3.6	75	5.5
NOTE: (2)	MEASURED	WITH EMI	INTERV	INSTALLED	IN LAUNCHER				

Q.A. ______________________

DATE: ______________________

ENGINEER Clayton E. Doggett
Robert E. [illegible]

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APPENDIX E

WORK AREA ENVIRONMENT

TITLE

MANUFACTURING AREA ENVIRONMENTS

1.0 SCOPE

1.1 Purpose: This standard establishes grades of cleanness for manufacturing, operating, testing, and storage environments, and requirements for controlling such grades.

1.2 Intended Use: Grades of cleanness are established for parts in process when non-contamination of the final product is mandatory.

1.3 Classification: Table 1 shows the six cleanness grades of area environments and the basic requirements for each.

2.0 APPLICABLE DOCUMENTS: The latest issue of the following documents, forms a part of this standard to the extent specified herein.

STANDARDS

Federal

FED-STD-209	Clean Room and Work Station Requirements, Controlled Environment

Military

MIL-STD-282	Filter Units, Protective Clothing, Gas Mask Components and Related Products, Performance Test Methods

FMC-DTL Manufacturing Process Control

MPC-2001	Solvent Cleaning
MPC-7001	Packaging and Material Handling

OTHER PUBLICATIONS

American Standards and Test Methods

Volume 8	Atmospheric Particle Counting Methods - F24, F25, F50

Society of Automotive Engineers

ARP-743	Procedure for Determination of Particulate Contamination of Air in Dust Controlled Spaces by Particle Count Method

Irving N. Sax Reinhold Publishing Company

Dangerous Properties of Industrial Materials

TABLE I

MANUFACTURING ENVIRONMENTS, MINIMUM REQUIREMENTS

The Requirements of the Highest-Grade Connected Atmosphere Shall Prevail(when separation is not complete)

	Clean Areas (Clean-Room or Clean-Bench)			Storage & Manufacturing		
GRADE:	2A (High)	2B (Medium)	2C (Low)	1A (High)	1B (Med.)	1C (Low)
Corresponding to: Type & Class - FED-STD-209 Class-	II, A Class 100	II, B Class 10,000	II, C Class 100,000	I, A None	I, B None	I, C None
Maximum Particle Count (Airborne), refer to Para. 4.3	100/ft^3, 0.5 microns and larger	65/ft^3, 5 microns and larger	700/ft^3, 5 microns and larger	100/cm^2, 10 microns and larger, in 1 hr. period	NR	NR
Filter Efficiency	99.97% for 0.3 micron particles			85%	*50%	NR
Temperature Setting	67-77°F, held within ± 0.5°F of set value			*72±3°F	*72±5°F	NR
Relative Humidity	45, -10%, +0%			*40±10%	*40±10%	NR
Air Press. Positive Differential	0.05 inches-of-water above any adjacent area			NR	NR	NR
Air Velocity	90 ft per minute (up to 1 inch from containing surfaces) +20 ft per minute in all unobstructed areas			NR	NR	NR
Ante-Room with Air-shower	Required for clothing storage and changing, personnel cleanup, and particle-generating cleaning processes			NR	NR	NR
Personnel Entering	Keep to minimum required for operation. Instruct thoroughly in clean-room requirements.			NR	NR	NR
Doors, Room	Double air-lock with air seals. Open door only when adjacent door is closed.			Air-Seal	Ordinary	Ord.
Doors, Bench, Pressurized	Air-sealed. Close as air pressure decays. Open after air pressure starts.			Same as Grade 2C	NR	NR
Surfaces of Room and Furnishings	Easily-cleaned and non-shedding, furniture shall not obstruct airflow any more than necessary			Same as Grade 2C	Clean & non-shed.	NR
Smoking, Food and Drink	Forbidden. Leave food and drink in outer area or ante-room.			Forbidden	Forbidden	Allwd.
Clothing	Lint-free smocks or coveralls. Low-lint clothing			Same as Grade 2C	Same as Grade 2C	NR
Head Covering	Lint-free head covering			Same as Grade 2C	NR	NR

TABLE I (Cont'd)

GRADE:	2A (High)	2B (Medium)	2C (Low)	1A (High)	1B (Med.)	1C (Low)
Corresponding to: Type & Class - FED-STD-209 Class-	II, A Class 100	II, B Class 10,000	II, C Class 100,000	I, A None	I, B None	I, C None
Lanolin-containing Soaps, Lotions, and Creams	Required (to prevent contamination with skin flakes)			Required	Req.	NR
Blowers	Start at least 15 minutes before area use.			Same as Grade 2C	NR	NR

NR = No Requirement. * = Unless authorized otherwise in work-control documents.

3.0 GENERAL

3.1 Safety: Minimum safety practices shall conform to the industrial safety regulations of the contractor's local, State, and Federal governments and to the contractor's safety code.

3.2 Handling and Packaging: Processed items shall be clean, or cleaned, and packaged before leaving the area. Cleaning shall conform to Standard MPC-2001. Packaging shall conform to Standard MPC-7001.

3.3 Grades of Area Environments: All storage and manufacturing areas shall conform to this paragraph and the work-control standard(s) shall designate the grade. Basic requirements of grades are listed in Table 1. Additional cleanness requirements are given in Section 4. A sign or label designating the area grade shall be placed on or beside the entrance in a conspicuous place, and shall state the basic requirements affecting personnel. Areas shall be designated as follows:

a) Grade 1C designates a general storage or manufacturing area of minimal requirements for machining, fusion welding, raw stock cutting, and rough assembly.

b) Grade 1B designates a general clean area for electronics assembling, manufacturing, and testing. It also designates a medium-grade storage area for parts and materials.

c) Grade 1A designates a high-grade clean area for special manufacturing processes and special testing of critical electronic parts or assemblies. It also designates a high-grade storage area for parts and materials.

d) Grades 2C, 2B, and 2A designate successively higher grades of super-clean areas for performing very critical manufacturing operations.

3.4 Equipment: The equipment used to control a manufacturing environment shall be capable of producing and maintaining the applicable environment grade. Equipment used to control, monitor, and record manufacturing area conditions shall be calibrated initially and as required by Quality Assurance.

3.5 Materials: The materials and processes, especially particle-generating operations, used in any manufacturing area shall not degrade the environment below the specified grade.

3.6 Definitions: Standard definitions apply except as noted otherwise.

3.6.1 Environments:

a) Manufacturing and Storage Area: A manufacturing and storage area environment is any continuous separately-contained atmosphere where products or raw materials are processed or stored. Separation may be by doors and/or differential air pressures.

b) Clean-Area: A clean-area environment is one in which pressure, humidity, air-borne particles, and temperatures are closely controlled to avoid degrading the product by contamination, corrosion, or temperature conditions.

c) Work-Control Documents: Work control documents are official documents that designate the work to be done (e.g., standards, engineering drawings, work orders, etc.).

3.6.2 Particle Size: The particle size is the maximum linear measurement of the particle expressed in microns (one millionth of a meter, 0.00003937"; about 25 microns equal 0.001"). The longest dimension of any fiber shall be taken as its particle size.

4.0 REQUIREMENTS

4.1 Additional Cleanness Requirements:

4.1.1 Personnel: Personnel allowed in Grade 1A or higher areas shall:

a) Prior to arrival at work, be wearing clean and approved clothing (no wool). Hair, face, hands and nails shall be completely free of spray, cosmetics, powder, polish, and creams or lotions containing silicones or other materials which could cause contamination.

b) After arrival at work, wash hands and face with soap and water before entering anteroom.

c) In the anteroom clean and vacuum clothing, air-shower, and put on clean lint free smocks, or coveralls, and head covering. (Ref. MIL-STD 282).

NOTE: Grade 1A areas do not require air-shower or head covering.

4.1.2 Tools and Parts: In Grade 1A, or higher areas:

a) Writing Materials shall consist of ballpoint pens and non-shedding paper. The use of lead pencils and erasers is forbidden.

b) Critical parts shall be handled with clean tweezers, gloves, or finger cots.

c) Tools and parts shall be covered with clean metal and/or plastic covers when not in use.

4.1.3 Benches, Equipment, Room Surfaces: In Grade 1B, or higher areas:

a) Clean work surfaces and tables daily. Use a clean cellulose sponge and detergents such as Wisk, Joy, or Ivory Liquid, then rinse surface with water.

b) Clean newly-acquired equipment by dusting, vacuuming, washing, or other suitable means before moving it into the manufacturing area or any anteroom.

c) Clean floors, walls, ceilings, and fixtures as necessary to conform to this standard. Floors shall be kept free of debris and shall be cleaned at least daily. Wall surfaces in all Grade 2 areas shall be cleaned at least weekly. All critical parts shall be covered, and facilities cleaned after work operations are ended.

d) Clean anterooms for changing clothes and eating according to standard good-housekeeping practices. Tables shall be cleaned daily. Floors shall be vacuumed daily and washed free of loose particles weekly.

4.1.4 Chemical Fumes: Concentration of fumes, such as those from acids, solvents, fluxes, potting compounds, and resin hardeners shall not exceed the Maximum Allowable Concentration (MAC) for any chemical, as specified in Dangerous Properties of Industrial Materials.

4.2 Work Positions: The more critical the operation, the closer it should be to the air filter outlet.

4.3 Air Analysis: The air in Grade 1A and higher areas shall be analyzed at least every two months, or as required by Quality Assurance, to insure compliance with this standard. Air-borne particles shall be monitored at each different representative location.

4.3.1 Grade 1A Areas: Monitor particles by the following dry-slide settling method (refer to ASTM F24):

a) Place clean dry glass slides in the selected locations for one hour.

b) Cover the slides, then use a microscope to count the number of particles larger than 10 microns.

c) If particle count is over 100 per square centimeter, take the necessary corrective action.

4.3.2 Grade 2 Areas: Monitor particles by one of the following methods, or other methods approved by Quality Assurance.

a) Light-Scattering Method: Draw the air sample into the optical test chamber of a scattered-light photometer. Each particle in the air scatters light into a photometer tube producing an electric current which is amplified and recorded. This method gives an arbitrary indication of the number and concentration of particles (refer to ASTM F50).

b) Filtration Method: Draw a measured air sample through a filter such as the Millipore Type AA Black Millipore (Millipore Filter Corporation, Bedford, Massachusetts). The collected particles are analyzed under a microscope for concentration and size distribution (refer to ASTM F25 or SAE ARP 743).

4.4 Relative Humidity: The relative humidity of an area shall be measured by use of a sling psychrometer (Taylor Instrument Co., Rochester, N. Y.), or a recording humidigraph Model 1HC500-40, or 4044 (Bristol Company, Waterbury, Conneticut) at intervals specified.

5.0 QUALITY ASSURANCE PROVISIONS

5.1 Approval: All Grade 1B or higher manufacturing areas shall be certified initially and as required by Quality Assurance to insure conformance to this standard. Certification tests shall consist of all of the tests in this standard, subject to final approval by Quality Assurance and any authorized customer representatives.

5.2 Calibration: Test instruments used for clean-room analysis shall be calibrated initially and as required by the Standards and Calibration Laboratory.

5.3 Surveillance: Surveillance shall be maintained by Quality Assurance to insure compliance with this standard.

FMC

APPENDIX F

SAMPLE CALIBRATION

PROCEDURES AND FORMS

ENGINEERING TEST SECTION
OPERATING PROCEDURE

NO: 1000 Rev. 8
DATE: 11 December 1973
PAGE: 1 of 7

ORDNANCE ENGINEERING DIVISION — SAN JOSE, CALIFORNIA

SUBJECT: CALIBRATION STANDARDS LABORATORY AND TEST EQUIPMENT STORAGE AND ISSUE CRIB

SUPERSEDES: 31 October 1973

A. PURPOSE:

To establish a uniform method for the calibration, maintenance and issue of measuring and test equipment owned by the Ordnance Engineering Division, and to establish requirements for records pertaining to such equipment.

B. GENERAL

1. The Calibration Standards Laboratory, under the direction of the Engineering Test Section, is responsible for calibration, maintenance and recording of all measuring and test equipment owned by OED. The calibration program is coordinated with, and responsive to the quality program in all areas of calibration control:

   a. Direct feedback from the Inspection Department provides prompt notification of damaged, uncalibrated, or malfunctioning test equipment utilized in acceptance testing.

   b. Audit reports from the Quality Assurance Department provide feedback on procurement, inspection, calibration, handling, usage, repair and storage of test equipment.

   c. All test work requests and test plans are reviewed for adequacy and utilization of proper test equipment; test results are evaluated and fed back to designers, vendors, customers, etc. as applicable.

   d. FMC Engineering Observer Reports, Equipment Performance Reports (EPR), Unsatisfactory Equipment Reports (UER), and other customer complaints are reviewed to determine adequacy of testing, equipment, etc.

   The above listed functions are performed by qualified test engineers and/or technicians as applicable to the task. The laboratory shall provide calibration service for other FMC divisions upon request on the basis of non-interference with OED requirements and reimbursement for time and material.

2. The Calibration Standards Laboratory shall maintain reference and transfer standards for calibration purposes, and shall ensure that reference standards are clearly traceable to recognized National Standards maintained at

the National Bureau of Standards or to accepted values of natural physical constants. Reference standards shall be maintained at 4 to 10 times better accuracy than transfer standards. Transfer standards used to calibrate measuring and test equipment shall be 4 to 10 times more accurate than the equipment being calibrated.

3. The Test Equipment Storage and Issue Crib, under the direction of the Engineering Test Section, shall be responsible for custody and checkout of instruments and equipment (except for calibration standards, instruments assigned to permanent locations, and those instruments requiring user qualification or instruction).

C. DEFINITIONS:

1. Measuring and test equipment - those instruments, meters, gages and other test devices used by qualified personnel for experimental measurements and product acceptance.
2. Reference Standards - highest order of accuracy standards retained in the Calibration Standards Laboratory to establish basic absolute values.
3. Transfer Standards - secondary measurement standards used to calibrate working equipment and other standards of lower accuracy.

D. FORMS:

1. Instrument Calibration and Issue Record - Form OED-409
2. Calibration Reports - Forms OED-360 and OED-487
3. Calibration Due Record - Form OED-515
4. Calibration Standards Laboratory Report of Calibration - Form OED-565
5. Pressure Gage Issue and Recall Record - Form OED-717.

E. PERSONNEL:

Personnel permanently assigned to the subject activities shall be evaluated by the Engineering Test Section Supervisor for ability to consistently produce results which comply with Government verification inspection. Permanent personnel shall include:

1. Supervising Test Engineer - A Test Engineer qualified by background and experience in electrical and electronic instrumentation shall supervise and be responsible for operation of the Calibration Standards Laboratory at all times. His functions shall include daily supervision of Laboratory personnel, engineering guidance as required, confirmation of accuracy, stability, and range of standards for intended use, and preparation and maintenance of current, written procedures for calibration and maintenance of all equipment serviced by the Calibration Standards Laboratory.
2. Technician - A qualified technician shall be permanently assigned to work in the Calibration Standards Laboratory under the direction of the Supervising Test Engineer.
3. Crib Attendant - The Test Equipment Storage and Issue Crib shall be manned by a Storekeeper or Crib Attendant under the guidance of an Engineer from the Engineering Test Section.

F. PROCEDURE:

1. Calibration Standards Laboratory shall:
   a. On receipt of new equipment items:
      (1) Calibrate each item in accordance with Para. b. below and establish a calibration interval for the item.
      (2) Prepare an Instrument Calibration and Issue Record (Form 409) for each item.

      NOTE: Form 409 will not be used for items to be issued permanently to specified areas of the plant.

      (3) Ensure that equipment bears a numerical identification, to be entered on all related records. In order of preference, this identification shall be the manufacturer's serial number, the FMC Property Accounting I.D. number or a number assigned by the supervising Test Engineer.
      (4) Forward the item and its instrument calibration and issue record card to the Test Equipment Storage and Issue Crib or to the permanent user.

b. Before placing new, rented or borrowed equipment in service, when required by calibration schedules, or whenever the need is apparent, calibrate equipment as follows:

(1) Calibrate against reference standards in accordance with applicable procedures and MIL-C-45662A. If equipment has been calibrated by an outside agency, Test Engineer shall determine adequacy of calibration and related documentation and, if adequate, may release equipment for use in accordance with this procedure.

NOTE: If it is impractical to move test instruments to the Laboratory for calibration, transfer standards may be used for calibration at the equipment site. Reference standards may not be removed from the laboratory except for recertification.

(2) Record each calibration on a Calibration Report form and maintain a file of all reports. Enter the calibration date in the appropriate section of the Instrument Calibration and Issue Record for each item. If calibration by another agency has been accepted, note Instrument Calibration and Issue Record accordingly.

(3) After calibration, affix a label to each test instrument identifying the calibrator and stating the date of calibration.

(4) Except as noted in (5) below, the next calibration due date shall be entered on the calibration label and Calibration Due Card by the Calibration Technician prior to return of the instrument to the Issue Crib.

(5) On most transducers and pressure gages (normal recall interval 2 months) the next calibration due date will be assigned at the time of issue by the Issue Crib Attendant or the Dynamometer Laboratory Leadman if gages are issued from the Dynamometer Laboratory. Recall intervals will be established by the Test Engineer and entered on the Pressure Gage Issue and Recall Record, Form OED-717.

c. If, on calibration, a test instrument fails to meet assigned specification requirements after repair or adjustment, the Test Engineer shall:

(1) Assign revised specifications, indicating the revision by a label of the test instrument and an entry in the instruction manual, or apply a "Limited Use" stamp to the calibration label and clearly identify the limitations.

d. Whenever an item of equipment is out of service for any reason, it shall be conspicuously identified with a label reading "NOT IN SERVICE-CALIBRATE BEFORE USING". So far as is practicable, out-of-service items shall be physically segregated from other equipment.

e. Whenever an indicating instrument is used in a manner where quantitative data or results are not required, the Test Engineer or the Calibration Technician shall conspicuously identify it with a label reading "INDICATION ONLY".

f. Maintain all measurement standards (reference and transfer) in a controlled environment. Temperature range shall be 68° to 76°F with no more than 1°F variation in any one hour period, and relative humidity shall be 30% to 60%. Cleanliness, vibration, and other controllable factors shall not adversely affect measurements. Reference standards shall be removed from this environment only for recertification in accordance with applicable procedures and the table of Appendix A. Transfer standards may be removed for use at equipment site in accordance with Para. b, above. Refer to Appendix B for a listing and calibration intervals of transfer standards.

g. Maintain certificates, reports and data sheets recording the dates, accuracy, and conditions under which reference standards have been calibrated. Documents shall identify higher echelon standards used and shall indicate traceability to recognized physical constants or National Standards. These records shall be available for inspection at any time.

h. Revise the calibration periods of test instruments in accordance with usage and demonstrated stability as determined from the records by the Test Engineer.

i. Extend calibration due dates for limited periods when test instruments are employed in urgent service. Users requesting such extensions shall later be notified of any out-of-specification conditions found when calibration is performed.

j. Issue special test equipment which is in the custody of the Calibration Laboratory. Make entry on Instrument Calibration and Issue Record (Form OED-409) each time equipment is issued or returned. Prepare Form OED-515 to cover equipment due for calibration. This applies both to items stored in the Instrument Crib and items stored in the Calibration Laboratory.

Recall items which are due for calibration. Items which are not readily moved or which require disassembly may be tagged with a "Not In Service-Calibrate Before Using" label.

2. Test Equipment Storage and Issue Crib shall:

a. Assign suitable shelf locations (Crib Item No.) for all equipment assigned for storage in the Instrument Crib. Issue measuring and test equipment to using personnel as requested. Perform a visual inspection for evidence of damage each time equipment is returned.

b. Make entry on Instrument Calibration and Issue Record (Form OED-409) each time equipment is issued or returned.

c. Enter next calibration due date on the label of pressure gages and transducers not used since last calibration. Due date shall be determined in accordance with the calibration interval assigned to the instrument by the Test Engineer and calculated from the date of first issue of the instrument following calibration. Make the appropriate entry on Form OED-717 and Form OED-409 for each pressure gage and transducer issued.

If a stock of calibrated but unassigned pressure gages is maintained in other locations, responsible personnel will enter the due date on the calibration label of each gage placed into service and make an appropriate entry on Form OED-717.

E. H. Suhr
Supervisor
Engineering Test

vm

ENGINEERING TEST SECTION
OPERATING PROCEDURE

NO: 1000 APP. A
DATE: 31 October 1973
PAGE: 1 of 1

ORDNANCE ENGINEERING DIVISION — SAN JOSE, CALIFORNIA

SUBJECT: CALIBRATION STANDARDS LABORATORY AND TEST EQUIPMENT STORAGE AND ISSUE CRIB
Appendix A

SUPERSEDES: 27 February 1973

REFERENCE STANDARDS

Parameter	Type Instrument Mfg. and Model	Serial	Calibration Interval	Calibration Source
Time and Frequency	Transmissions of WWV, Fort Collins, Colorado continuously available.			
Electrical Voltage	Standard Cells	686595 724619	1 year	Simco Electronics
	Eppley Type 100	783712		
Electrical (Resistance)	General Radio Co. Type 1440-9631 Standard Resistor 10KΩ	9741	3 years	General Radio
	Leeds & Northrup 4020-B 1.0 ohm	1795443	3 years	Leeds & Northrup
(Capacitance)	General Radio Co.		5 years	General Radio
	Type 1409-9712,.01MF	15715		
	Type 1409-9720,0.1MF Standard Capacitors	15371		
Pressure	Deadweight Tester Ashcroft 1305-B	1 BA 03925	As required*	Ashcroft Corp.
			5 years	Weights: SC County Dept. of Weights & Measures
Sound Level	Bruel & Kjaer Model 4220 Pistonphone	227276	As required*	Bruel & Kjaer Cleveland, Ohio
Temperature	Platinum Resistance Thermometer Rosemount 104MB48ACCA	62103	2 years	Rosemount
	Linear Bridge Rosemount 414L	2796	2 years	Rosemount
Illuminance	Tektronix J16 Digital Photometer	B020303	6 months	OED Calibration Lab.
	J6501 Probe	B010238	1 year	Tektronix Corp.

*Calibration is based on physical dimensions. Recalibration is only required when visual inspection indicates wear.

ENGINEERING TEST SECTION
OPERATING PROCEDURE

NO: 1000 APP. B
DATE: 31 October 1973
PAGE: 1 of 1

ORDNANCE ENGINEERING DIVISION — SAN JOSE, CALIFORNIA

SUBJECT: CALIBRATION STANDARDS LABORATORY AND TEST EQUIPMENT STORAGE AND ISSUE CRIB
Appendix B

SUPERSEDES: 27 February 1973

TRANSFER STANDARDS

Parameter	Type Instrument Mfg. and Model	Serial	Calibration Interval
Time Frequency	Electronic Counter Hewlett-Packard 5300A/5304A	1212A00933	6 months
Electrical DC Voltage	Universal Potentiometer Leeds & Northrup K3 Model 7553	1309288	18 months
	Volt Box L & N 7582	1560894	18 months
AC and DC Voltage and Current	Meter Calibrator Hewlett-Packard 6920B	7D1091	6 months
	Digital Voltmeter Non-Linear Systems MX-1	.532	6 months
DC Current	L & N K3 and Shunt Box L & N 4385	1598013	1 year
AC Frequency Response	Hewlett-Packard Thermal Converter 11050A	416-00442	Note 1
AC and DC Attenuation	Decade Attenuator General Radio 1450TBR	1984	1 year
AC and DC Voltage Ratio	Voltage Divider General Radio 1454A	3343	1 year
Resistance	General Electric Portable Double Bridge 9069199G1	CDB1	1 year
	General Radio Co. Type 1432-P Decade Resistor	28126	1 year
Temperature	Jos. Kaye Co. Model 2110 Ice Point Reference Standard	7335	1 year

NOTES:

1. Calibration not required. Certified by type and construction.

FMC

CALIBRATION DUE

MONTH _____ CRIB ITEM NO. _____

1	2	3	4	5	6	7	8	9	10	11	12	

MONDAY

1	2	3	4

INTERVAL _____

DESCRIPTION _____

MODEL OR P/N _____

LOCATION _____

OED-515 (3-69)

TYPE _____ MFG & MODEL _____ S/N _____

RANGE _____ CALIB PROCEDURE _____ INTERVAL _____

CAL DATE	DUE DATE	ISSUED TO	DATE OUT	DATE IN	ISSUED TO	DATE OUT	DATE IN

OED-409 (9-68) INSTRUMENT CALIBRATION AND ISSUE RECORD

FMC Ordnance Engineering Division
San Jose

REPORT OF CALIBRATION
Calibration Standards Laboratory

Instrument _____

Manufacturer & Model _____ S/N or ID _____

This certifies that the above instrument conforms to original manufacturer's specifications unless otherwise noted. Calibration was accomplished at a temperature of 72°F. Records of all final testing are maintained at the OED Calibration Standards Laboratory and are available for inspection.

The calibration of this instrument has been accomplished by comparison to standards traceable to national standards maintained by the National Bureau of Standards.

Date Tested: _____ Date Due: _____ Tested By: _____

Remarks:

OED-565 (3-74)

FMC

ORDNANCE
ENGINEERING
DIVISION
SAN JOSE CALIFORNIA

CALIBRATION REPORT

1. STANDARDS LABORATORY
2. SUBMITTING ACTIVITY
3. TEST INSTRUMENT *(Item Calibrated)*
4. MANUFACTURER
5. MODEL NUMBER
6. SERIAL NUMBER

7. REASON FOR SUBMISSION
   - CERTIFICATION 1
   - CALIBRATION 2
   - CROSSCHECK 3
   - OPERATIONAL FAILURE 4
8. DATE OF LAST SERVICING
   - CERTIFICATION 1
   - CALIBRATION 2
   - CROSSCHECK 3

1. CALIBRATION PROCEDURE
2. CALIBRATION TECHNICIAN
3. TEST DATE
4. TEMPERATURE -°F
5. RELATIVE HUMIDITY

1. TEST INSTRUMENT EVIDENCED
   - GOOD CONDITION 1
   - SEVERE ENVIRONMENT 2
   - PHYSICAL MISHANDLING 3
   - AGE AND LONG SERVICE 4
   - OVERLOAD 5
2. TEST INSTRUMENT FOUND
   - OUTSIDE ADJUSTMENT TOLERANCE 1
   - WITHIN ACCEPTANCE TOLERANCE 2
   - OUTSIDE ACCEPTANCE TOLERANCE 3
3. TEST INSTRUMENT RETURNED
   - OUTSIDE ADJUSTMENT TOLERANCE 1
   - WITHIN ACCEPTANCE TOLERANCE 2
   - OUTSIDE ACCEPTANCE TOLERANCE 3
4. CERTIFICATED OR REPORTED VALUE, IF FIXED STANDARD
5. MAN-HOURS TO CALIBRATE
6. MAN-HOURS TO ADJUST OR REPAIR

CALIBRATION EQUIPMENT
(LIST ALL EQUIPMENT USED IN THIS CALIBRATION)

MANUFACTURER	MODEL NO.	SERIAL NO.	RECALL DATE	MANUFACTURER	MODEL NO.	SERIAL NO.	RECALL DATE

REMARKS

OED-360 8-68

CALIBRATION DATA

PROCEDURE STEP NO. (1)	FUNCTION TESTED (2)	READING OR VALUE		CORRECTED VALUE OF COLUMN ___ (5)	ALGEBRAIC ERROR (6)	CALIBRATION TOLERANCES		READING AFTER ADJUSTMENT (9)
		NOMINAL (3)	MEASURED (4)			ACCEPTANCE (7)	ADJUSTMENT (8)	

OED-360-1 (8-68)

CALIBRATION REPORT

ORDNANCE ENGINEERING DIVISION
SAN JOSE, CALIFORNIA

ITEM _____ ID# _____ RANGE _____ CALIBRATE AT _____ CARDINAL POINTS

LOCATION USED _____ ACCEPTANCE ± _____

NOMINAL CALIBRATION POINT	CAL DATE: / DUE DATE: / TECHNICIAN: / STD: / TEMP: °F / HUMIDITY: %		CAL DATE: / DUE DATE: / TECHNICIAN: / STD: / TEMP: °F / HUMIDITY: %		CAL DATE: / DUE DATE: / TECHNICIAN: / STD: / TEMP: °F / HUMIDITY: %		CAL DATE: / DUE DATE: / TECHNICIAN: / STD: / TEMP: °F / HUMIDITY: %		CAL DATE: / DUE DATE: / TECHNICIAN: / STD: / TEMP: °F / HUMIDITY: %		CAL DATE: / DUE DATE: / TECHNICIAN: / STD: / TEMP: °F / HUMIDITY: %		NOMINAL CALIBRATION POINT
	AS REC'D	AS ISSUED	AS REC'D	AS ISSUED	AS REC'D	AS ISSUED	AS REC'D	AS ISSUED	AS REC'D	AS ISSUED	AS REC'D	AS ISSUED	
ZERO													ZERO
UPSCALE													
DOWNSCALE													
ZERO													ZERO

OED-487 (3-69)

FMC

APPENDIX G

MOLD INSERT PULL TEST

FMC Central Engineering Laboratories
Santa Clara
756-342-828 CEL

MATERIALS LABORATORY TEST REPORT

Lab No: 760859

C[illegible] No:	015-400-000	Part Name: Solid State Switch	Part No:
Date:	2-11-76		Lot Size:
Req By:	Dean Andrus	Heat No:	P.O. No:
Phone:	3342	Size:	Rec. No:
Div/Plt:	0ED	Mfgr:	No. Test Pcs:

Specification:

Information Desired:

☐ Conformance of Material to Specification
☐ Conformance of Certification to Specification
☐ Process Analysis, Bath/Panel Conformance
XX Other — Explain

Force required to pull out three mounting screw inserts. Please identify the three.

Results: 2-18-76

Insert*	Force
#1	635 lbs.
#2	390 "
#3	592 "

* See Figure 1 for position of insert.

Rick Brown

Rick Brown

def

CEL 626 (4-75)

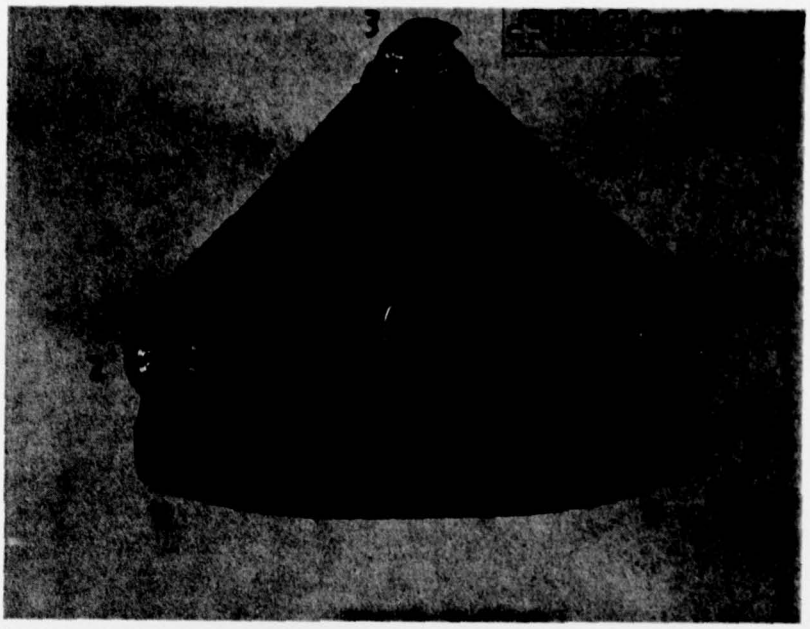

Figure 1. Solid State Switch MAG=2X

Note: The numbers refer to the results given above.